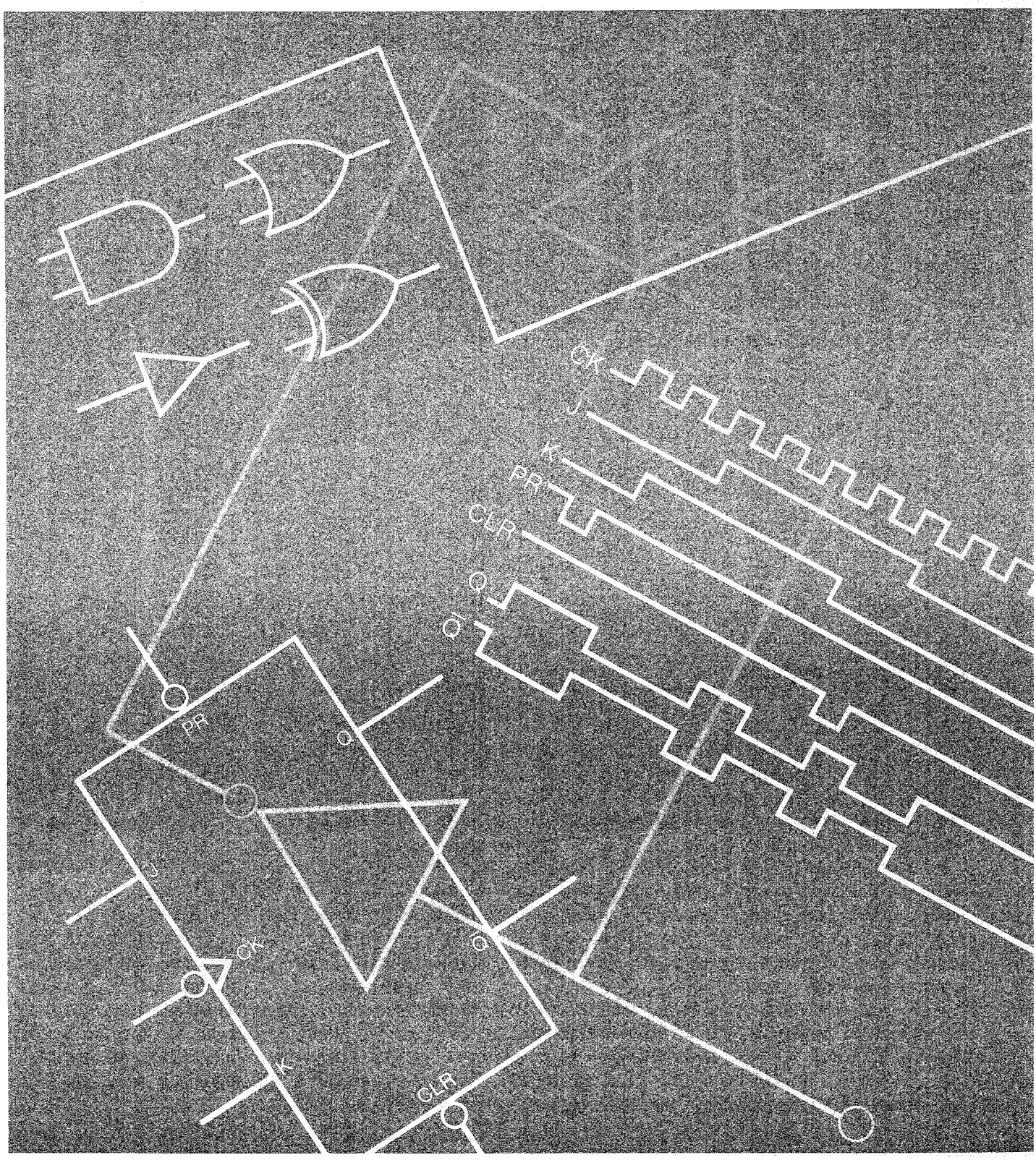
DIGITAL

PIONEER

SUPPLEMENT OF TUNING FORK



Dear Readers

The word "digital" is by no means new to you. "Digital" has been used to describe many things, from clocks to computers. It's as though the mere mention of the word created a spell-binding effect. No wonder sales promotion ad agencies make frequent use of the word!

In fact, today, digital technology has made its presence felt among audio products such as tape decks, turntables, tuners, etc. As a result, the products' features and functions as well as their quality and reliability have been greatly improved over conventional versions.

For instance, many relays and switches have been replaced by digital IC's which use the simple logic of 0 and 1, or ON and OFF in a pair. In control circuits, digital IC's have been employed for auto music selection, auto lead-in, return and repeat functions, etc. In Pioneer's high-end digital tuner, for example, digital technology has also been employed for automatic scanning, programmable preset tuning, electronic switching, LED and LCD display circuits and stable frequency performance.

There is no doubt that many new products to be released in the near future will make greater use of digital IC technology. With this in mind, Pioneer has prepared this book to help you understand the fundamental digital principles and to supplement the explanations in service manuals for Pioneer products featuring digital technology.

There are many things to be learned before acquiring a complete understanding of "digital," and it is our hope that this book will be helpful in your study.

Contents

Basic Course "Digital"

1. Digital and analog

The quantity of countable things, like trees or cars, can be determined by counting them digitally. On the other hand, uncountable things, such as water or time, must be measured analogically to determine their volume. Digital data is comprised of discrete units which have no intermediate value. If medium quantity is undesirable or inconvenient, digital processing is very effective.

The ordinary household light switch and thermostat whose positions or values are changeable in discrete steps, are digital circuits.

Diodes and transistors also work as digital switches.

2. Logic circuit

In a logic circuit, the numbers 1 and 0 are used. These numbers in themselves do not indicate values but opposite states, such as "yes" and "no," "on" and "off," or "high" and "low." By using 1 and 0, the shifting process of all logic circuits can be understood and expressed in a logical algebraic form. (See appendix on Boolean Algebra.)

2-1. Types of circuits

a) NOT circuit (Inverter)

NOT circuits are shown in Fig. 1 (a) and (b).

When the input of the circuit becomes 1, the output becomes 0, and when the input becomes 0, the output becomes 1 as shown on the truth table in Fig. 1 (c).

The circles in the symbols indicate negation, which will be explained later.

The function of a NOT circuit can be expressed algebraically by $F = \bar{A}$, $\bar{A}$ standing for negative A.

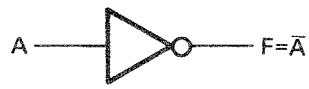
The lamp circuit shown in Fig. 1 (d) illustrates a simple example of a NOT circuit.

Supposing that:

Switch A is closed: A = 1
Switch A is open: A = 0
Lamp is on: F = 1
Lamp is off: F = 0

Then, as the circuit clearly shows, the switch is open when the lamp is on. This proves that A and F are reversed as in the truth table in Fig. 1 (c).

(a) Symbol 1



(b) Symbol 2

(c) Truth table

A	F=Ā
1	0
0	1

(d) Light switching circuit

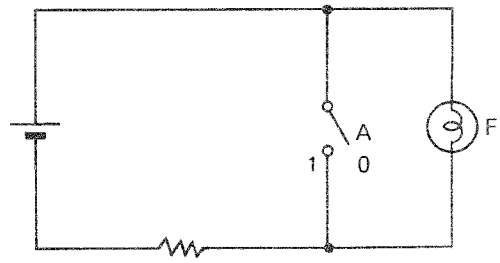


Fig. 1 NOT circuit

b) AND circuit (Logical multiplication)

A typical AND circuit is shown in Fig. 2.

With two inputs, there are four combinations. Since the output becomes 1 only when the inputs are 1, the function can be expressed by $F = A \cdot B$.

Now let's apply this to the lamp circuit.

The lamp will go on only when both A and B are 1. This can be determined by multiplying A and B as shown in the Fig. 2 (b) truth table.

Such a relationship between A and B is called logical multiplication, or AND, and such a circuit is known as an AND circuit.

(a) Symbol

(b) Truth table

A	B	F=A·B
0	0	0
0	1	0
1	0	0
1	1	1

(c) Light switching circuit

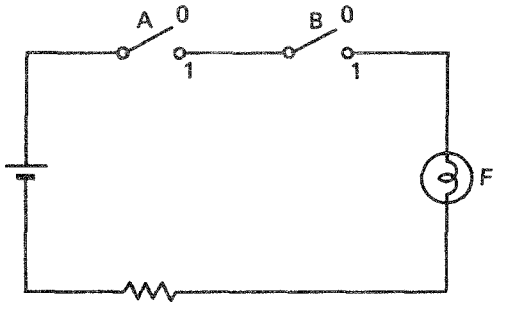


Fig. 2 AND circuit

c) OR circuit (Logical addition)

This type of circuit is illustrated in Fig. 3.

With this circuit the output becomes 1 when at least one input is 1.

This function is expressed as $F = A + B$.

Applying this to the lamp circuit in Fig. 3 (c), the lamp will be on when A or B is 1. In other words, this is determined by adding A and B as shown in the truth table in Fig. 3 (b).

(a) Symbol

(b) Truth table

A	B	F=A+B
0	0	0
0	1	1
1	0	1
1	1	1

(c) Light switching circuit

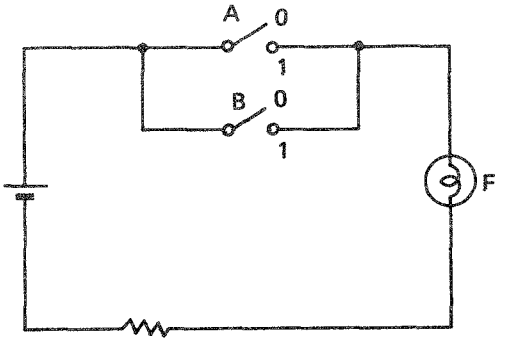


Fig. 3 OR circuit

d) NAND circuit

A NAND circuit is shown in Fig. 4.

This is a combination of an AND circuit and a NOT circuit.

As output F is the reverse of the AND circuit's output A·B, it is represented by $\overline{A \cdot B}$, the symbol for which is shown in Fig. 4 (b).

The truth table in Fig. 4 (c) indicates that output F is the reverse of AND.

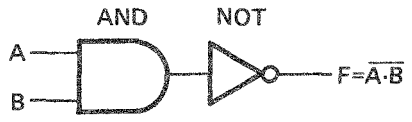
e) NOR circuit

Fig. 5 shows a NOR circuit, which is a combination of an OR and a NOT circuit.

As output F is the reverse of the OR circuit's A + B output, it is represented by $\overline{A + B}$, the symbol for which is shown in Fig. 5 (b).

The truth table in Fig. 5 (c) indicates that output F is the reverse of OR.

(a) Function



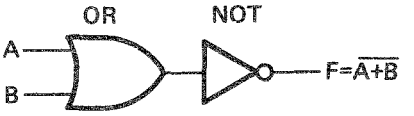
(b) Symbol

(c) Truth table

A	B	F=$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 4 NAND circuit

(a) Function



(b) Symbol

(c) Truth table

A	B	F=$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 5 NOR circuit

2-2. Positive and negative logic

A logic circuit sounds very complicated. But Pioneer products already have circuits such as the one shown in Fig. 6. Since years ago, when the words "digital circuit" were not popular, we have been reading conventional circuits in the logical way.

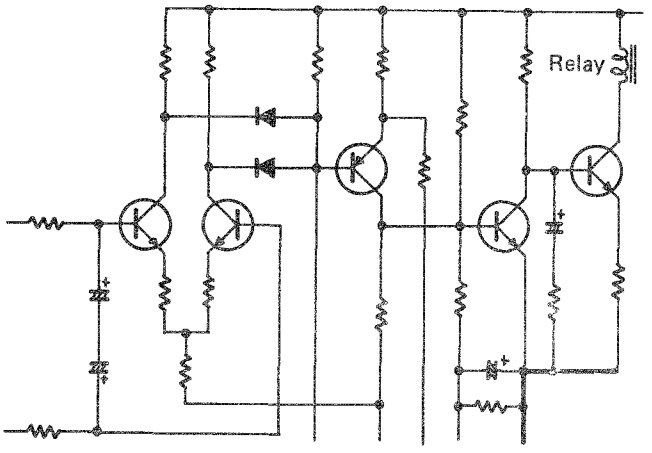


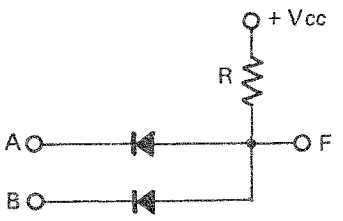
Fig. 6 Typical protection circuit

When the voltage level at the base of a NPN (PNP) transistor becomes high, the level at the collector becomes low (high). Fig. 7 shows part of the protection circuit in Fig. 6, while Fig. 7 (b) shows its function table.

When both input levels become high (Vcc : supplied voltage), the output level becomes high. When these high and low (0V) levels correspond to 1 and 0 respectively, this circuit becomes an AND circuit, Fig. 7 (c). When these high and low levels correspond to 0 and 1 respectively, the function becomes that of an OR circuit, Fig. 7 (d). The logical function of a circuit changes completely when the level correspondents are shifted. The former (H = 1 and L = 0) is called "positive logic" and the latter (H = 0 and L = 1), "negative logic."

The circles at the terminal of Fig. 7 (d) indicate negative logic. Circuit (d) is an Invert NOR type, having negation circles at both input and output.

(a) Part of protection



(b) Function table

A	B	F	
L	L	L	H≒Vcc
L	H	L	L≒0V
H	L	L	
H	H	H	

(c) For positive logic

A	B	F=A·B
0	0	0
0	1	0
1	0	0
1	1	1

(d) For negative logic

$\bar{A}$	$\bar{B}$	$F=\overline{\bar{A}+\bar{B}}$
1	1	1
1	0	1
0	1	1
0	0	0

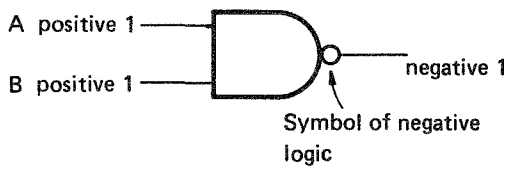
Fig. 7 Logic circuit

When positive logic 1 is applied to the input of the NOT circuit in Fig. 1 (a), the output becomes negative logic 1. The NAND circuit in Fig. 8 (a) can be considered an AND circuit with positive input logic and negative output logic. The circuit is the same as that shown in Fig. 4 (b).

Then positive logic 1 is applied to inputs A and B, the output becomes negative logic 1. When the output of the above is expressed in negative logic, the truth table will be the same as that of an AND circuit. Why should the same level be regarded differently? The answer is that it is easy to understand a whole circuit when the state of "lighting lamp" or "rotating motor" is expressed as 1 in Fig. 9 where the positive logic AND circuit shows that the lamp lights when the output is 0, which is hard to understand..

In Fig. 10, it is expressed with the negative logic Invert NOR circuit. With this circuit, it is easier to understand the function (refer to Fig. 11) that causes the lamp to light when one of the inputs is 1 (negative logic). The fact that a circuit can be considered to function as either an AND circuit or an OR circuit by positive or negative logic respectively is called "logical relativity."

(a) NAND positive logic input
negative logic output

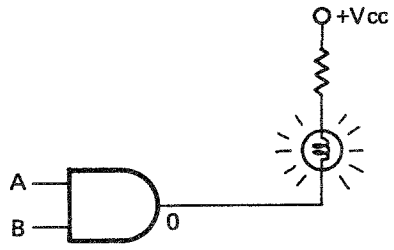


(b) Truth table

Positive logic		Negative logic
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 8 NAND circuit

(a) For positive AND circuit application

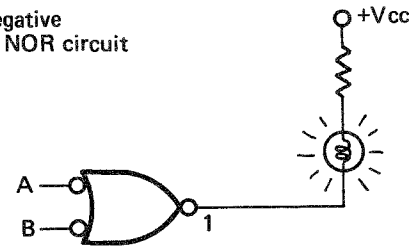


(b) Truth table

A	B	Output	
0	0	0	ON
0	1	0	ON
1	0	0	ON
1	1	1	OFF

Fig. 9 AND circuit

(a) For negative
Invert NOR circuit



(b) Truth table

A	B	Output	
1	1	1	ON
1	0	1	ON
0	1	1	ON
0	0	0	OFF

Fig. 10 Invert NOR circuit

These examples explain why there is both positive and negative logic for the same function.
Then, what about actual repair of a product or checking its operation? In this case, H (high) and L (low) levels are used, rather than the truth table, for checking voltage and wave forms.
The numbers 1 and 0 are useful when considering digital circuits logically, but a function table is more convenient for repairing.
Now let's see how the functions of each logic circuit can be easily understood from a circuit diagram that contains negative logic symbols.
In Table 1, the positive logic can be represented by H and the negative logic (marked with o) by L. So let's use a NAND circuit (positive logic input) and an Invert OR circuit (negative logic input) and see what happens.

(1) NAND circuit

As the input is positive logic, it is represented by H; and the output, negative logic, by L. As the symbol is NOT + AND (AND + NOT), F = L when A and B = H. This is represented by

A	B	F
H	H	L

in the function table.

(2) Invert OR circuit

As the input is negative logic, it is represented by L, and the output, positive logic, by H. As the symbol is NOT + OR, F = H when A or B = L. This is represented by

A	B	F
L	L	H
L	H	H
H	L	H

in the function table.

Thus, a part of the function is represented by a symbol. As these logic circuits are generally termed gates, we will refer to them as such from here on (a NAND circuit = a NAND gate).

Table 2 shows various gates most frequently used. Please refer to 4-3i for the Exclusive OR circuit explanation.

Positive logic input	Negative logic input	Function table
A = H, F = H A — F Buffer	A = L, F = L A — F Buffer	A | F L | L H | H
A = H, F = L A — F Inverter	A = L, F = H A — F Inverter	A | F L | H H | L
A and B = H, F = H A, B — F AND	A or B = L, F = L A, B — F Invert NOR	A | B | F L | L | L L | H | L H | L | L H | H | H
A or B = H, F = H A, B — F OR	A and B = L, F = L A, B — F Invert NAND	A | B | F L | L | L L | H | H H | L | H H | H | H
A and B = H, F = L A, B — F NAND	A or B = L, F = H A, B — F Invert OR	A | B | F L | L | H L | H | H H | L | H H | H | L
A or B = H, F = L A, B — F NOR	A and B = L, F = H A, B — F Invert AND	A | B | F L | L | H L | H | L H | L | L H | H | L

Table 1 Conversion table

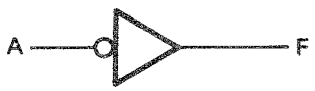
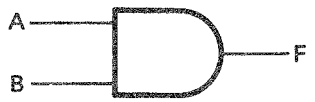
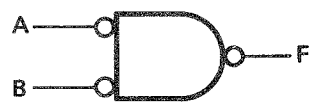
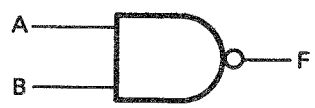
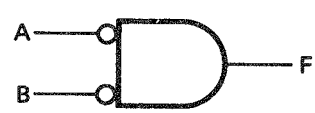
Positive logic input	Negative logic input	Function table
 Buffer F=A	 Buffer F=A	A | F L | L H | H
 Inverter F=$\overline{A}$	 Inverter F=$\overline{A}$	A | F L | H H | L
 AND F=A·B	 Invert NOR F=$\overline{A}+\overline{B}$	A | B | F L | L | L L | H | L H | L | L H | H | H
 OR F=A+B	 Invert NAND F=$\overline{A}\cdot\overline{B}$	A | B | F L | L | L L | H | H H | L | H H | H | H
 NAND F=$\overline{A\cdot B}$	 Invert OR F=$\overline{A}+\overline{B}$	A | B | F L | L | H L | H | H H | L | H H | H | L
 NOR F=$\overline{A+B}$	 Invert AND F=$\overline{A}\cdot\overline{B}$	A | B | F L | L | H L | H | L H | L | L H | H | L
 Exclusive OR F=A$\overline{B}$+$\overline{A}$B =A⊕B	 Inclusive NAND F=$\overline{A\overline{B}+\overline{A}B}$	A | B | F L | L | L L | H | H H | L | H H | H | L
 Exclusive NOR F=$\overline{A\overline{B}+\overline{A}B}$ =$\overline{A\oplus B}$	 Inclusive AND F=A$\overline{B}$+$\overline{A}$B	A | B | F L | L | H L | H | L H | L | L H | H | H

Table 2 Gate variations

3. Digital IC's

3-1. Types of digital IC's

Digital IC's can be classified by structure as follows: bipolar type using transistors and unipolar type using MOS FET's.
These two types can be further broken down into:

(a) Bipolar type

*RTL (Resistor-Transistor Logic)
Old type not in use now.

*DTL (Diode-Transistor Logic)
Scarcely used now.

*TTL (Transistor-Transistor Logic)
The current mainstay type.

*ECL (Emitter-Coupled Logic) or CML (Current Mode Logic) an expensive, high-speed type.

*I^2L (Integrated-Injection Logic) or MTL (Merged-Transistor Logic)
A super-high-speed, high-density type.
Expected to be the future mainstream type.

(b) Unipolar type

*PMOS (P-channel MOS FET)
This was used in early-type LSI (large scale integration). It is still used in custom-made LSI's.

*NMOS (N-channel MOS FET)
Widely used in present-day LSI.

*CMOS (Complementary MOS FET)
Most widely used at present in various components from ordinary gates to custom-made LSI.

The bipolar type generally responds quickly, though it consumes a considerable amount of power, while the unipolar type has a relatively slower response time and consumes less power. Since audio equipment does not require high speed, the less power consuming unipolar type is widely used.
As bipolar IC's are mostly TTL type and unipolar mostly CMOS type, these two will be explained in detail here; the others we will leave for another occasion.

3-2. Density of integration and packages

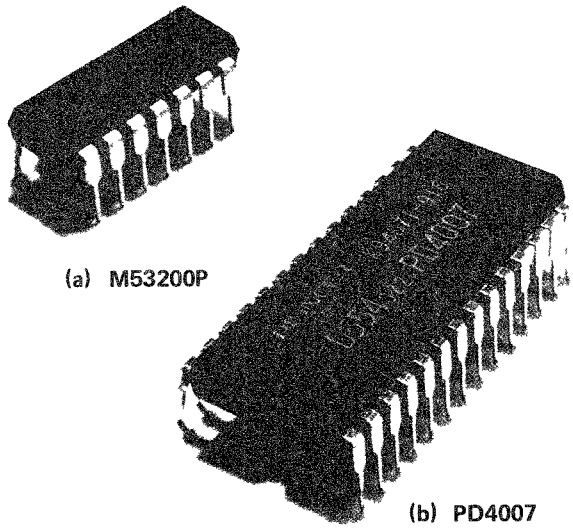
As the number of elements (the number of gates) contained in a single package differs widely, IC's are classified by the density of integration of their elements. However, this classification is not rigid, differing from maker to maker.

a) SSI (Small Scale Integration)
Number of elements: Less than 100
Number of gates: Less than 12

b) MSI (Medium Scale Integration)
Number of elements: 100 or more and less than 1,000
Number of gates: 12 or more and less than 100

c) LSI (Large Scale Integration)
Number of elements: 1,000 or more
Number of gates: 100 or more

As for the package, digital IC's used in audio products are mostly plasticmolded DIP (dual-inline package) type. The photo (a) shows a NAND gate TTL IC with 14 terminals (14P), while (b) illustrates a 28P custom-made CMOS IC.



(a) M53200P

(b) PD4007

There is also a flat type, which is widely used in watches and clocks, as well as for industrial and military applications.
A gate IC contains several gates within a single package.

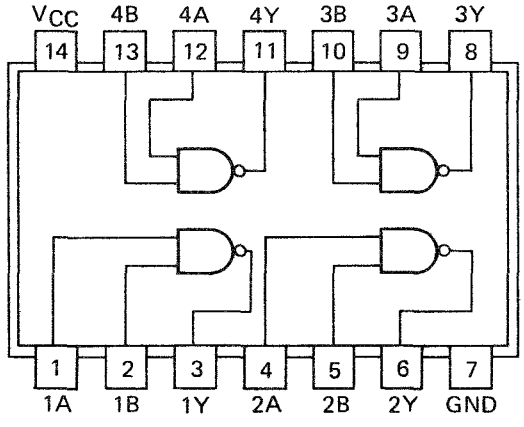


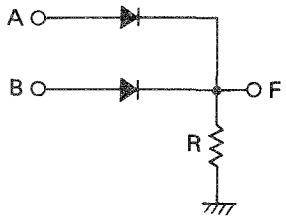
Fig. 11 SN7400N pin assignment (top view)

TTL IC Primary Course — Threshold level

A circuit with two diodes and a resistor has logic functions. The circuit depicted in Fig. A (a), which is similar to that in Fig. 7 (a), functions as an OR gate by positive logic and as an INVERT NAND gate by negative logic. Threshold voltage level for shifting from 1 to 0 or 0 to 1 is determined by the forward rising voltage characteristics of a diode. But, actually, the level varies gradually [Fig. B] and no threshold can be found even if the input impedance is 0 and output load impedance is infinite. There would be no problem if a discrete level of 0V or Vcc were applied to the input. But, when gates are connected in series [Fig. C], the combined circuit does not function.

Even when the input of the gate 1 is 0V, the output of Gate 3 becomes 2.1V (0.7V + 0.7V + 0.7V). The minimum voltage required to make a current run through a diode is about 0.7V. The more stages, the harder it is to function as shown in Fig. C. With the circuit of Fig. D (a), a high input level of 5V decreases down to 2.9V at output. When threshold level is not discrete, logical judgement of 1 or 0 becomes difficult if the number of stages increases. The ideal input-output characteristics of an AND or OR gate are shown in Fig. E. The output voltage should change when the input becomes Vcc/2 and the difference between high and low levels should be large at input.

(a) Circuit



(b) Symbol

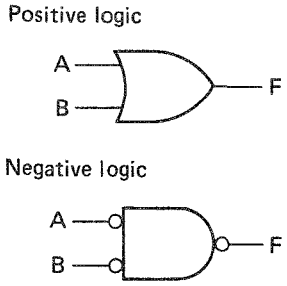


Fig. A Logic circuit with diodes and a resistor

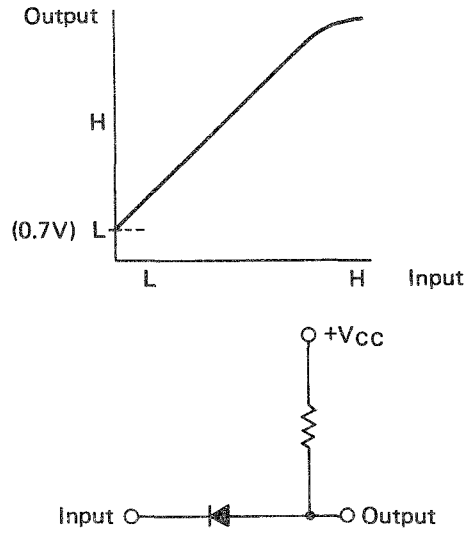
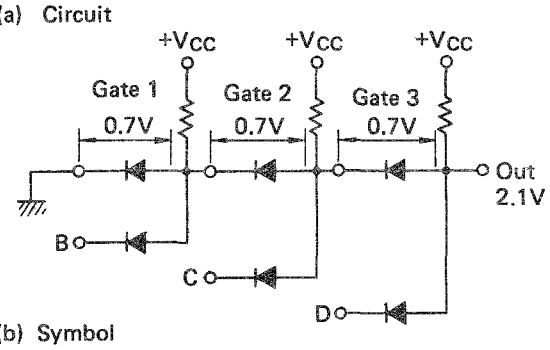


Fig. B Input-output characteristics of a gate made of a diode and a resistor

(a) Circuit



(b) Symbol

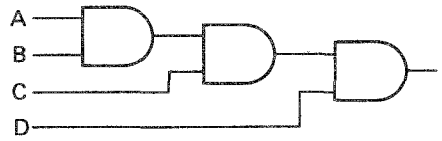
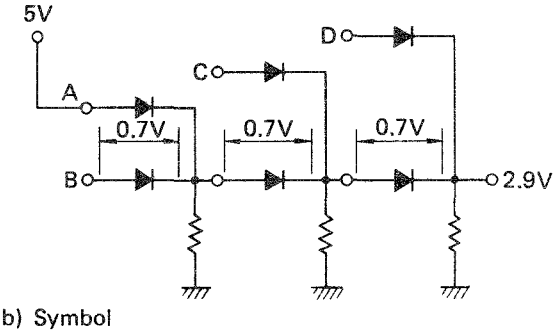


Fig. C Gate connection in series

(a) Circuit



(b) Symbol

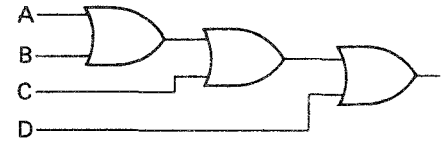


Fig. D Gate connection in parallel

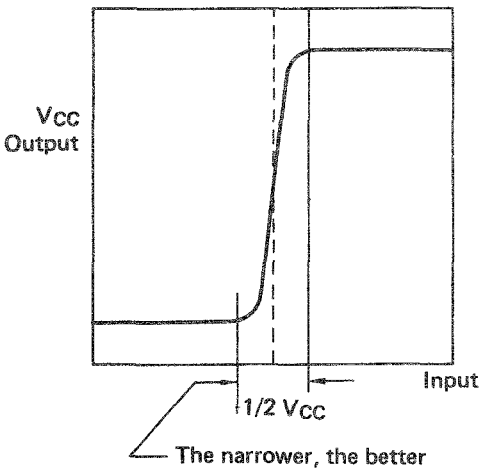


Fig. E Output-input characteristics

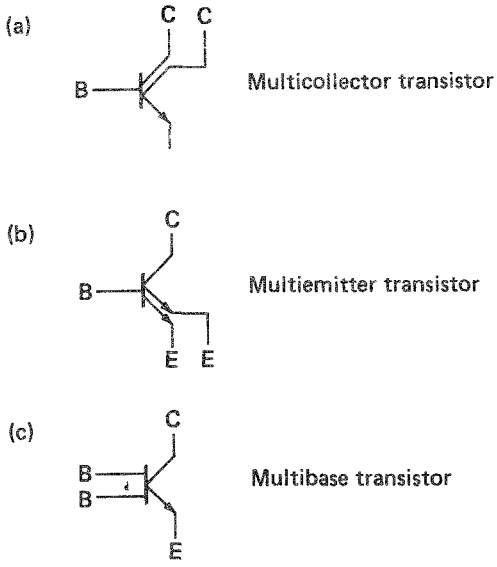


Fig. G Multi-transistor

As you see, there are problems with gates which are made of diodes and resistors. To overcome the ambiguous threshold and output level differences between H and L, RTL, DTL, TTL, etc. have been developed utilizing transistors for switching functions. However, a gate has other characteristics such as delay time or response time and FAN OUT or the number of gates which can be connected to a single output. Today, TTL's are more popular for these applications. Fig. F is the circuit of a TTL NAND gate. In the figure you see an unfamiliar transistor Q_1. This is called a "multiemitter transistor"; one of the multi-transistors shown in Fig. G, it is often used in digital and analog IC's. Its equivalent circuit is shown in Fig. H.

Input/output voltages of TTL IC's should be remembered when checking circuits which employ TTL IC's, or checking IC circuits will be impossible. Refer to Fig. 15.

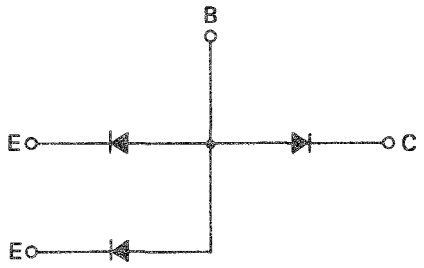


Fig. H Equivalent circuit of multiemitter transistor

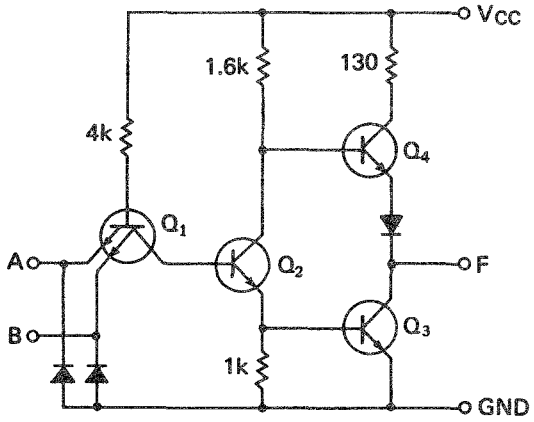


Fig. F Basic circuit of TTL NAND gate

3-3. TTL IC

The original source of a TTL IC is the SN74 series circuit of Texas Instruments (TI). Currently, semiconductor makers are producing IC's with similar standards as second sources.

This chapter will deal with the standard type. For your reference, the following table shows their power consumption per gate and propagation delay time.

Type	Power consumption	Propagation delay time
74 (Standard)	10mW	10nS
74L (Low power)	1mW	40nS
74H (High speed)	22mW	6.5nS
74S (Schottky)	19mW	3nS
74LS (Low-power Schottky)	2mW	10nS

Table 3 Power consumption per gate/propagation delay time

Now let's go into the electric characteristics of TTL IC's.

a) Absolute maximum ratings

These are the maximum values permissible. Any change in condition which increases the stipulated value, even if it is instantaneous, will cause breakdown or deterioration of the TTL IC.

Supply voltage:	7V
Input voltage:	−0.5 ~ +5.5V
Storage temperature range:	−55 ~ +150°C

b) Recommended operating condition

This is the necessary condition for obtaining the following performance.

	Min.	NOR	Max.
Operating supply voltage (V):	4.75	5	5.25
Fan-out*:			10
Operating temperature (°C):	0	25	70

*Fan-out: The number of parallel-connected gates that can be driven by a single gate.

c) Electrical characteristics

(1) Input voltages

This is the voltage limit which can maintain output logical states (H or L).

H level input voltage V_{IH}: 2V (min.). This is the minimum input voltage level which can maintain positive logic output of L.

L level input voltage V_{IL}: 0.8V (max.). Maximum input level which can maintain positive logic output of H.

(2) Input current

This is the input current at the time Vcc max. is applied to the input.

The current varies in proportion to that of the supply voltage.

H level input current I_{IH}: 40μA (max.)

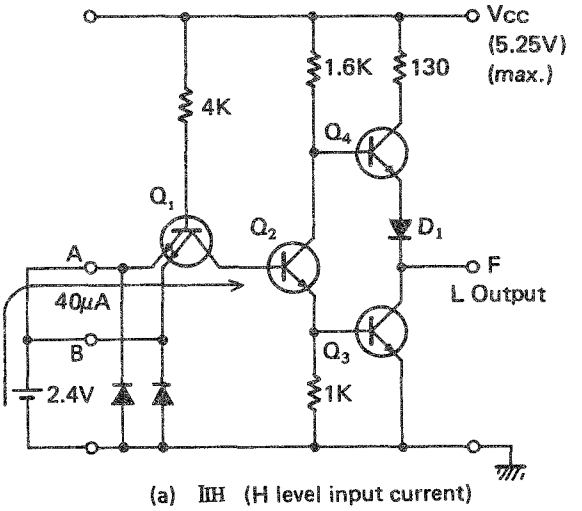
Condition: Vcc = (max.) V_{IN} = 2.4V

L level input current I_{IL}: −1.6mA (max.)

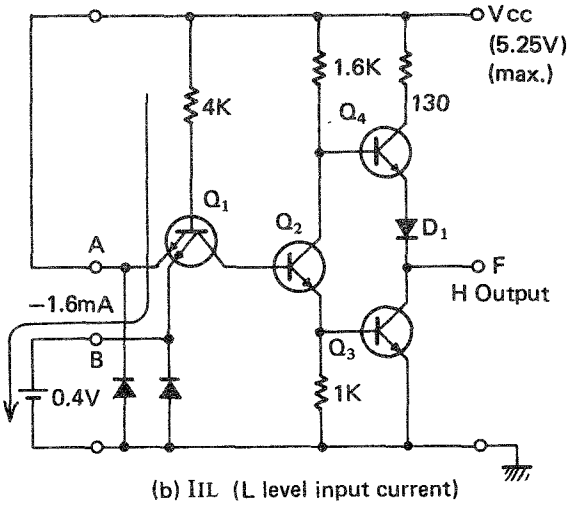
This (−) symbol means that the current is flowing out.

Condition: Vcc = (max.), V_{IN} = 0.4V

Fig. 12 shows the input current measuring conditions. Under these conditions, the input current is at its max.



(a) I_{IH} (H level input current)



(b) I_{IL} (L level input current)

Fig. 12 Measuring condition of input current

(3) Output voltages

These also vary according to the power supply voltage (4.75 ~ 5.25V). It is the value of the time when the minimum operatable supply voltage is applied, because when the supply voltage decreases, the transistor base current decreases and this occurs even when the output is L, making it difficult to keep the state of the transistor saturated.

H level output voltage V_{OH}: 2.4V (min.), 3.3V (TYP)*

Condition: V_{CC} = (min.); V_{IN} = 0.8V, I_{OH} = −400μA

L level output voltage V_{OL}: 0.4V (max.), 0.22V (TYP)

Condition: V_{CC} = (min.); V_{IN} = 2.4V, I_{OL} = 16mA

Fig. 13 shows the measuring condition which makes the output voltage worst, or minimum, and indicates the direction of the output current.

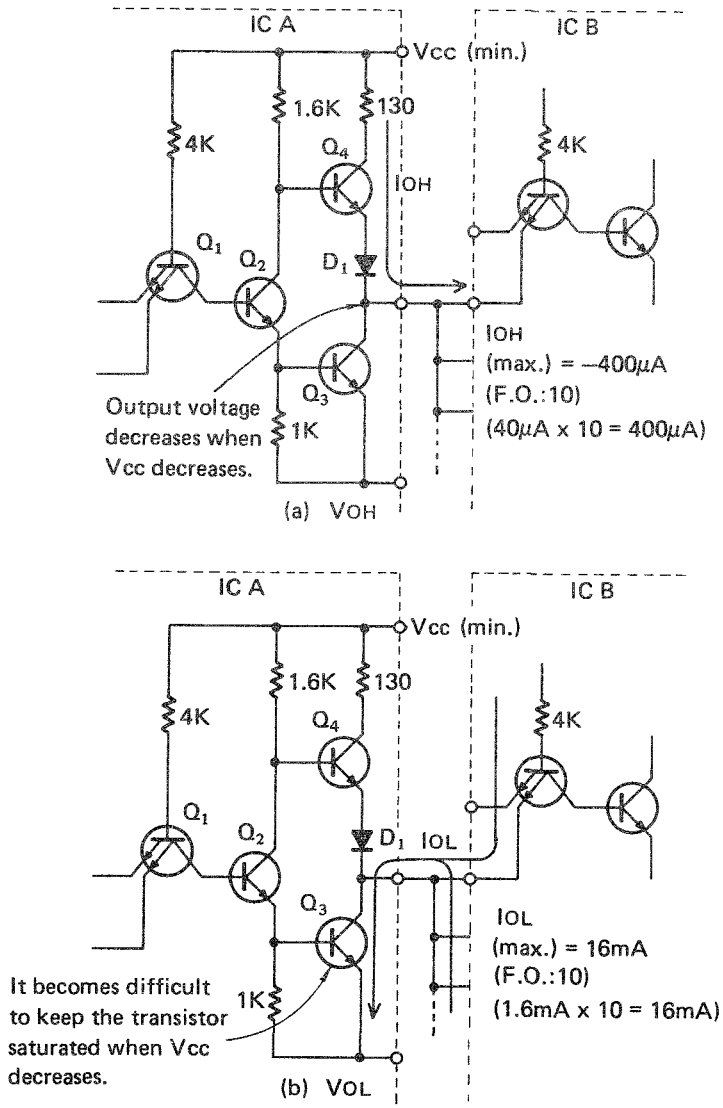


Fig. 13 Measuring condition of output voltage

(4) Propagation delay time

The propagation delay time of a TTL IC is determined by the inner circuit being free from external interference. That of a NAND gate SN7400 is 10ns. The most influential load capacitance to produce a time delay of 6ns/100PF is determined by the following formula.

Propagation delay time: $t_{pd} = (10 + 0.06C_L)$ns

C_L : load capacitance (pF)

(5) Power consumption

The power consumption of a gate is 5mW when the output level is H, and 15mW when it is L. This makes the average 10mW.

(6) Input/output characteristic

The input/output voltage characteristic of a TTL IC is shown in Fig. 14. The threshold voltage at a normal temperature T_A of 25°C will be around 1.3V.

* TYP stands for typical value.

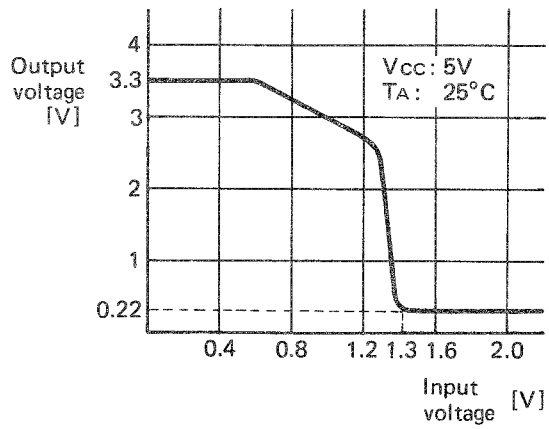


Fig. 14 Characteristic of input voltage vs. output voltage

Fig. 15 shows the input/output voltage range of a TTL IC.

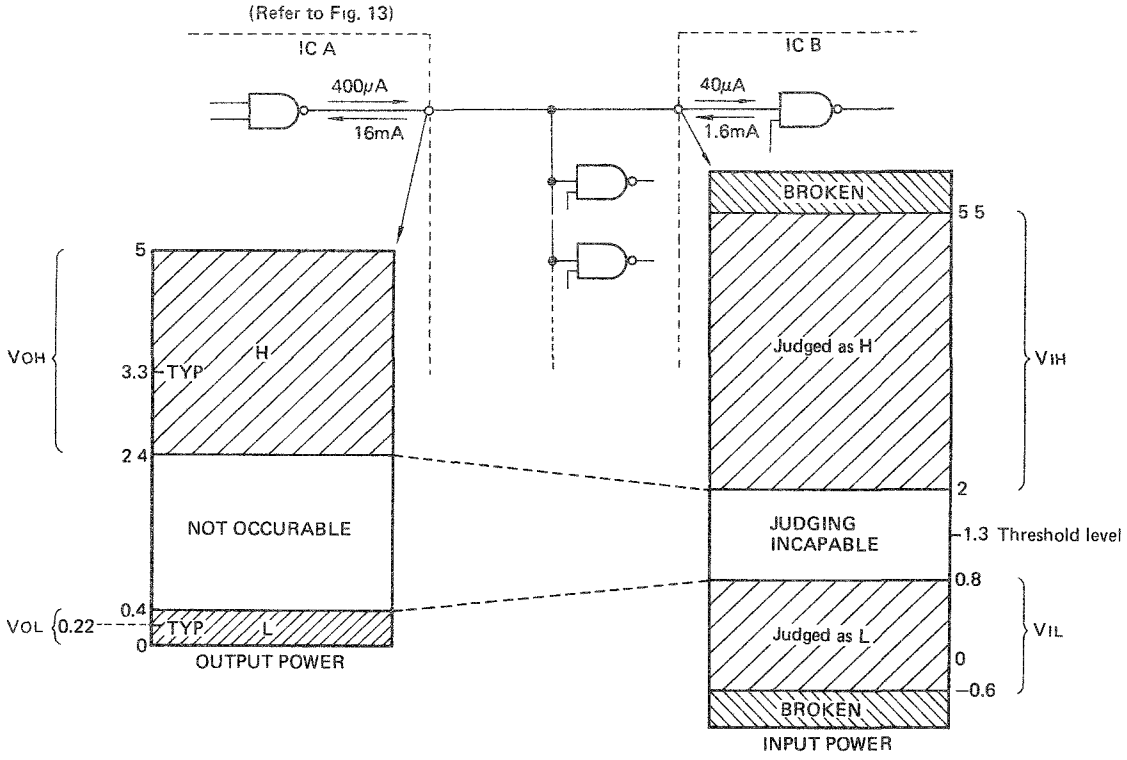


Fig. 15 Voltage range of input and output of TTL IC

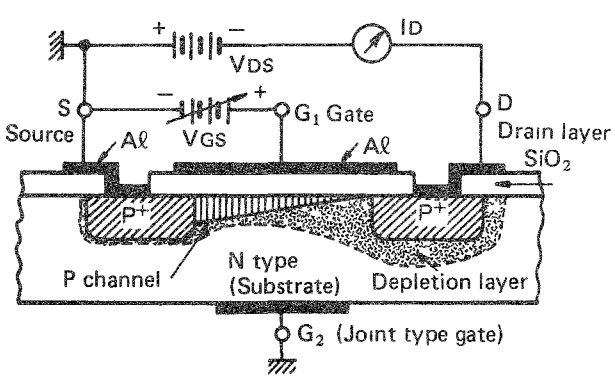
3-4. CMOS IC (Complementary Metal Oxide Semiconductor IC)

a) MOS-FET

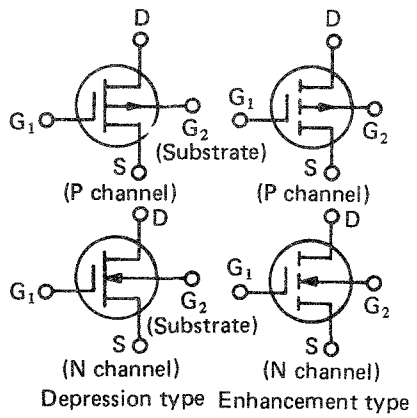
Transistors currently being used are bipolar and FET type. The former is simply called "transistor," being used in popular amplifiers or TTL IC's. The latter can be subdivided into JFET (junction type, popularly employed in low-noise amplifiers) and MOS type. The MOS type consists of aluminum, SiO_2 and a semiconductor as shown in Fig. 16. Resistance between drain and source can be controlled in the range between $10^2\Omega$ (ON) and $10^{10}\Omega$ (OFF) by varying the voltage between the gate and source and by varying the current channel width.

The differences between the bipolar type transistor and MOS FET's are:

Bipolar transistor	MOS FET
(1) Base current flows.	Base current is very small because of insulated gate. Voltage-controlled type.
(2) Saturation voltage remains.	When ON, drain and source are in ohmic contact. No saturation voltage remains.



(a) Type structure & bias method (P channel)



(b) Circuit symbols

Fig. 16 Structure of MOS FET

b) CMOS logic circuit

In MOS FET's, there are P-channel and N-channel complementary types just like bipolar transistors. An IC which has both P-channel and N-channel MOS FET's on one substrate is called a CMOS IC. How, then, can we combine CMOS FET's in composing a logic circuit?

Fig. 17 shows an inverter which is a fundamental CMOS logic circuit.

Fig. 18 shows its input/output and power supply current characteristics.

Note that the threshold is about 1/2VDD, "L" and "H" levels are 0V and VDD respectively and I flows only when the input voltage is around the threshold voltage. You will find that the characteristics of a CMOS inverter differ a little from those of a TTL IC.

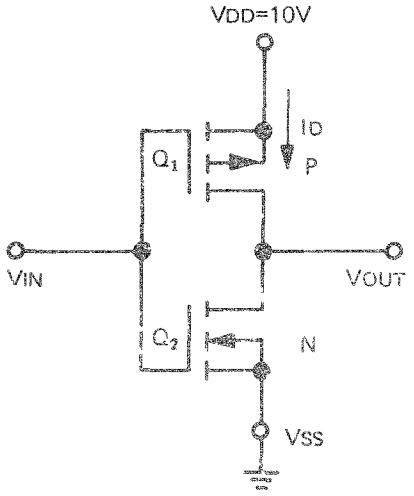


Fig. 17 CMOS inverter

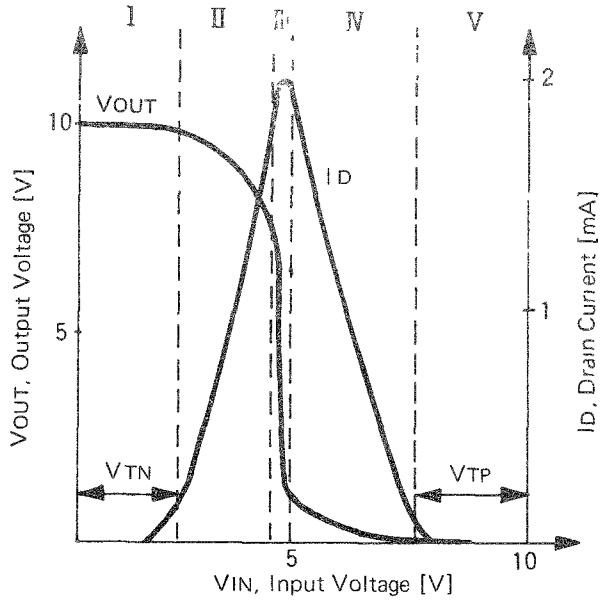


Fig. 18 CMOS inverter characteristics

Fig. 19 shows the input-output characteristics of CMOS inverter under various supply voltages. The threshold is always about 1/2VDD.

Then how can we make NOR and NAND gates?

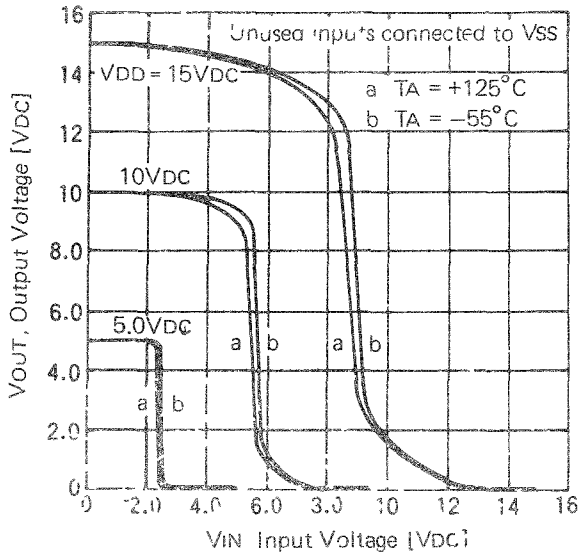
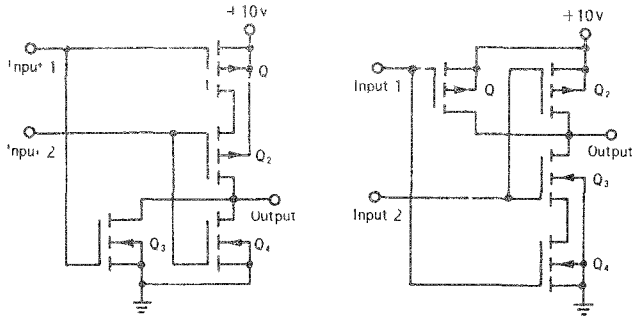


Fig. 19 Input/output characteristics of CMOS inverter under various voltage supplied

Fig. 20 shows fundamental 2-input NOR and 3-input NAND gates. FET's with the same polarity can be piled up without resistors because MOS FET leaves no saturation voltage while it is ON. The inputs can be increased by piling the FET's up. Table 4 shows the function of the NOR gate of Fig. 20 (a). Q_1, Q_2, Q_3 and Q_4 each works as a switch.



(a) 2-Input NOR Gate (b) 2-Input NAND Gate

Fig. 20 Fundamental circuit of CMOS gate

Table 4 Action of 2-input NOR gate

"L" = 0V "H" = +10V

Input 1	Input 2	Q_1	Q_2	Q_3	Q_4	Output
L	L	ON	ON	OFF	OFF	H
L	H	ON	OFF	OFF	ON	L
H	L	OFF	ON	ON	OFF	L
H	H	OFF	OFF	ON	ON	L

c) CMOS and TTL

CMOS and TTL are the same from the viewpoint of their logic circuits, but differ in the following points. Fig 21 shows that the power consumption of CMOS gate is very low (about 1/100 that of a TTL gate) at low frequency. Its I_D is about 10^{-9}A when its output remains unchanged. The power increases in proportion to frequency because the crossing frequency of fluctuating voltage through the threshold in a certain period of time increases. Power consumption is important for battery-operated systems. By minimizing heat generation, the integration of large-scale circuits and further increasing of reliability are possible. CMOS gates can be operated in the wide power supply range of 3 ~ 18V, while TTL gates function only within the range of 5V ±0.25V.

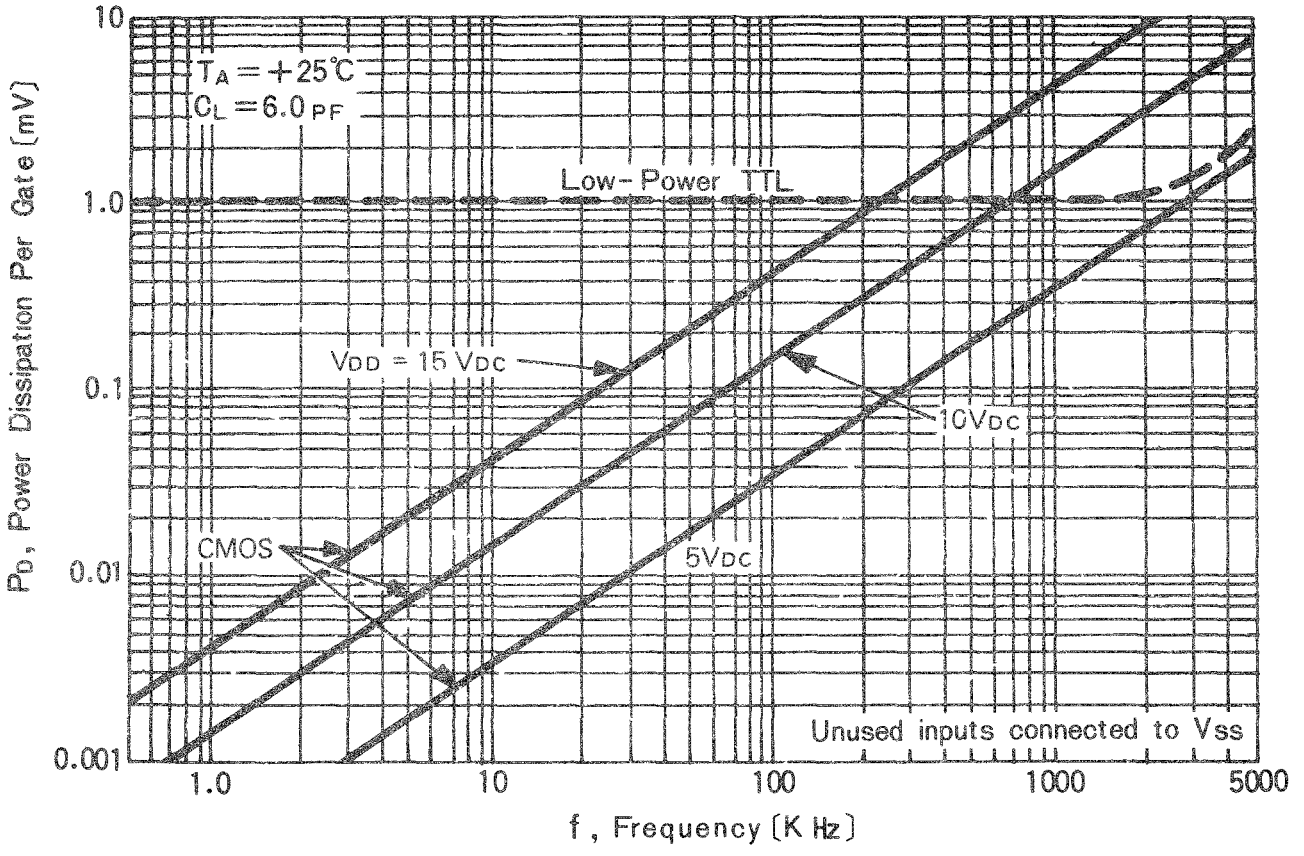
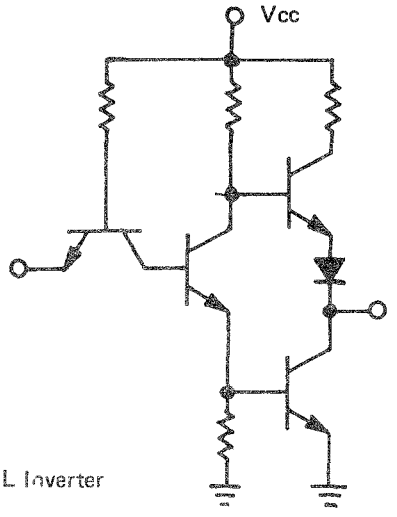


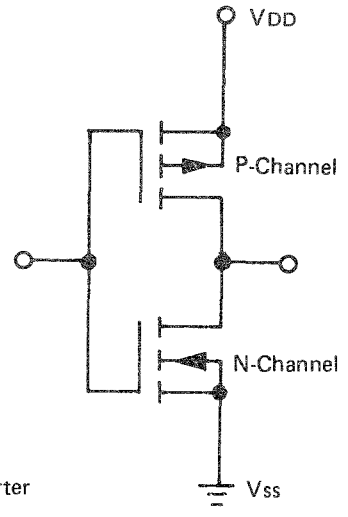
Fig. 21 Power consumption of CMOS gate

CMOS gates have a large noise margin because their threshold is always about 1/2 of the power supply voltage and their logic levels are almost the same as the power supply voltage or the ground level. The noise margin of a CMOS gate is about 45% of the power supply voltage while that of a TTL gate is about 1V. CMOS gates have more than 50 terminals for Fan-outs because input current is negligible, while TTL gates of the same family have about 10. However, the number of Fan-outs that can be provided is limited due to wave deformation.

CMOS IC's usually don't employ resistors because transistors can be substituted and are easily integrated into IC's. One slight disadvantage of CMOS gates is their slow response time. The propagation delay time of the MC14001B is 100nS (V_{DD} = 5V) while that of the Texas Instrument's TTL SN7400 is 10nS. So, CMOS gates are operated with a comparatively low clock frequency of about 100kHz.



TTL Inverter



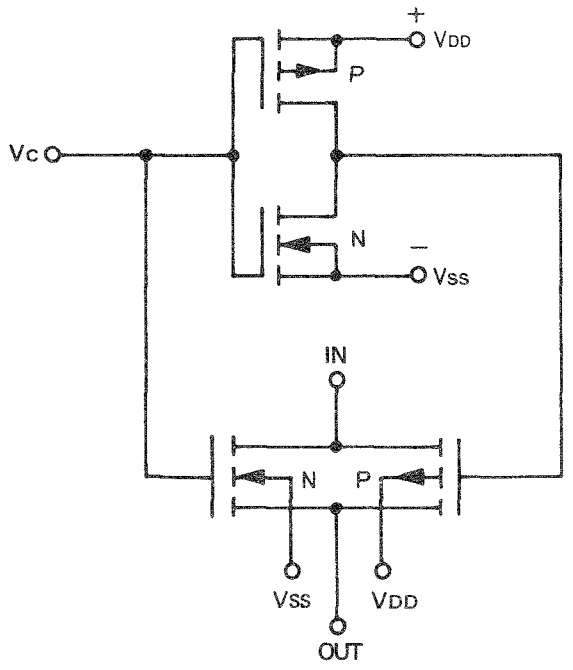
CMOS Inverter

Fig. 22 TTL and CMOS Inverters

d) CMOS switch

A MOS-FET is ideal except for the fact that this has a relatively low maximum input voltage. Fig. 23 shows a bi-directional CMOS switch. When H level voltage is fed to Vc, the contact between IN and OUT becomes ON, having a resistance of about $10^2\,\Omega$ in both directions. When Vc is at L level, it becomes OFF permitting some current leakage. With this switch, many circuits can be simplified.

(a) Equivalent circuit



(b) Circuit symbol

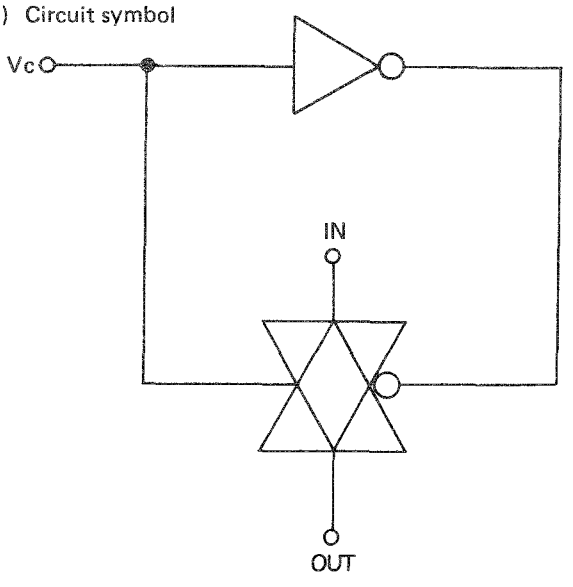


Fig. 23 CMOS switch

e) Cautions in CMOS IC use

The CMOS IC is electrostatically weak. When it was introduced into the market, it was easily damaged by even rubbing it with a piece of cloth or by operating a piezoelectric cigarette lighter nearby. Because its gate is electronically isolated, being insulated by a thin 1,000Å foil, a leaking AC line voltage generated by a soldering iron may destroy the IC. For protection, the IC should be kept on a piece of conductive sponge or wrapped properly in a piece of aluminum foil.

These conditions apply to NMOS and PMOS IC's. Special care should be taken when handling LSI's, as these are expensive components.

4. Gate combinations

4-1. Advantages of invert-gate circuits

There are many IC's such as NAND and NOR which use inverted logic. Such invert gates are useful when combined with other gates, although they are a little difficult to understand. The main advantage of invert gates is their simplicity. Fig. 24 shows NAND and AND gate circuits. You will see how few elements a NAND gate requires, how little power it consumes and how short its propagation delay time is.

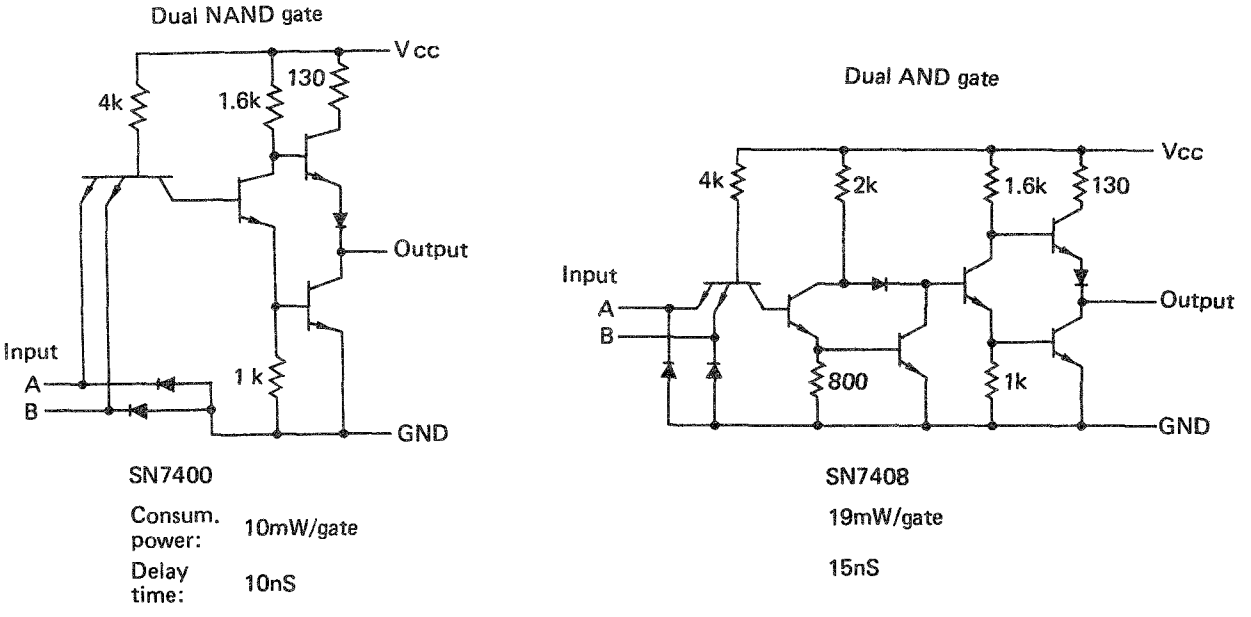


Fig. 24 Circuit of NAND and AND gates

4-2. Multistage gate connections

When gates are to be connected with many steps, it is better to connect them so that power consumption at each step is as low as possible and the total power consumption is kept to a minimum. In addition, from the standpoint of propagation delay, it is better to compose a circuit with invert gates.

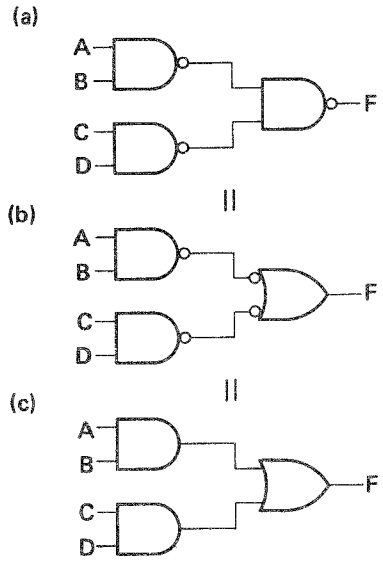


Fig. 25 NAND gate combinations

It is easier to understand the logic structure of a circuit if the NAND gates at the output are expressed as Invert OR so that the logic between the steps are made consistent with negative logic.

If the logic throughout a circuit is consistent, whether it is positive or negative, the results will be the same. However, it is also possible for a circuit to use combined logic as in an AND and OR circuit.

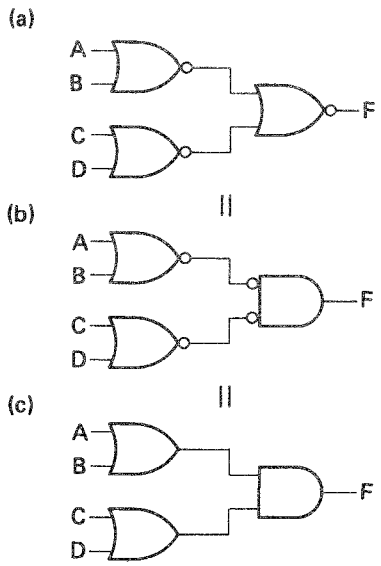


Fig. 26 NOR gate combinations

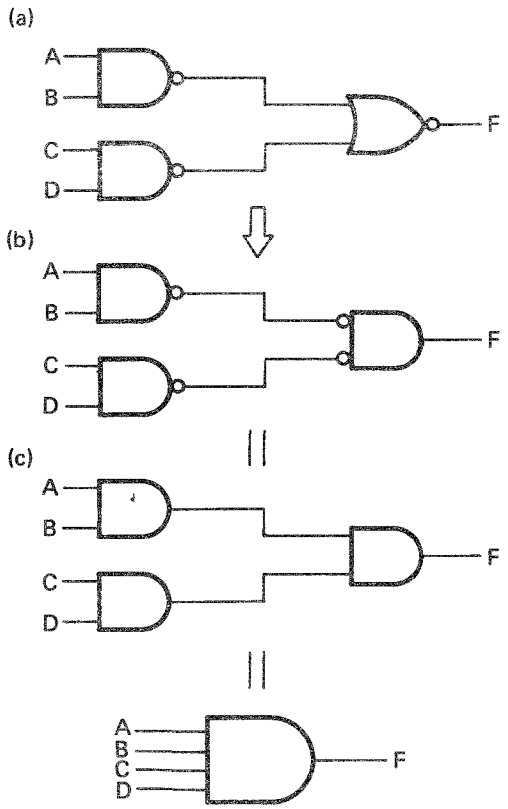


Fig. 27 NAND-NOR connections

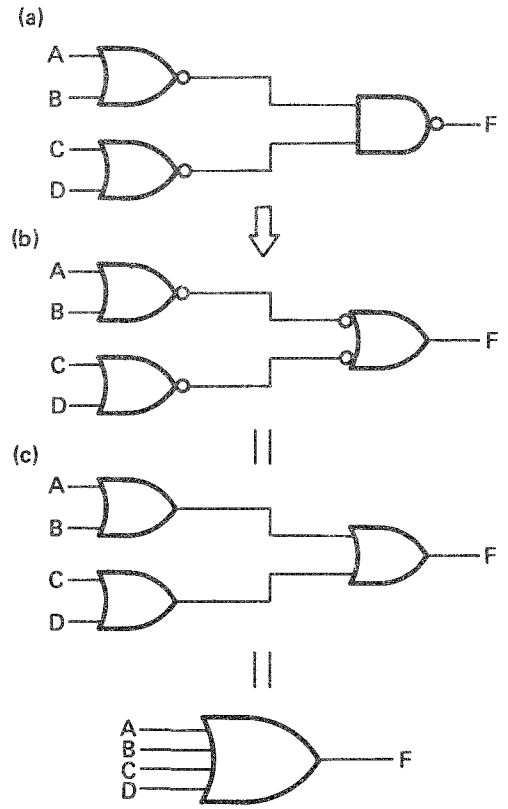


Fig. 28 NOR-NAND connections

4-3. Circuit employing gates

a) NAND and NOR gates as inverters

Fig. 29 shows one method for making an inverter using NAND and NOR gates. The NAND and NOR truth tables on page 3 explain why they can become an inverter.

This method makes full use of an IC. If a circuit requires three NAND gates and one inverter, it can be made with a NAND IC, which usually consists of four NAND gates, by making a NAND gate into an inverter.

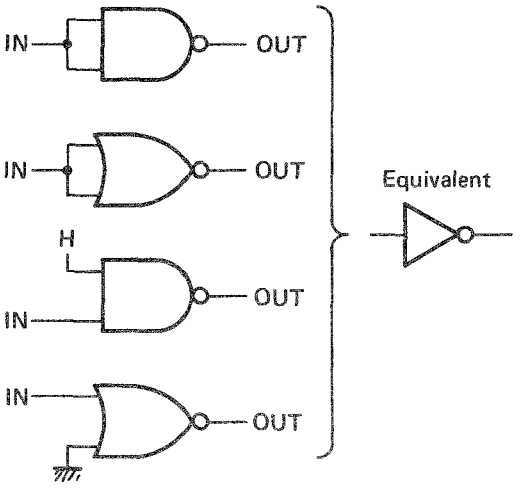


Fig. 29 Using NAND-NOR gate as inverter

b) Delay circuit

This circuit uses the charging and discharging time of capacitors for delaying output-signal-to-input-signal response. The delay time is determined by the time constant of C (capacitor) and R (resistor).

In Fig. 30 (a), the time from H to L and from L to H will be delayed in both cases. In (b), the time from H to L will be delayed, however, there will be no time delay from L to H since C is discharging through a diode and not R.

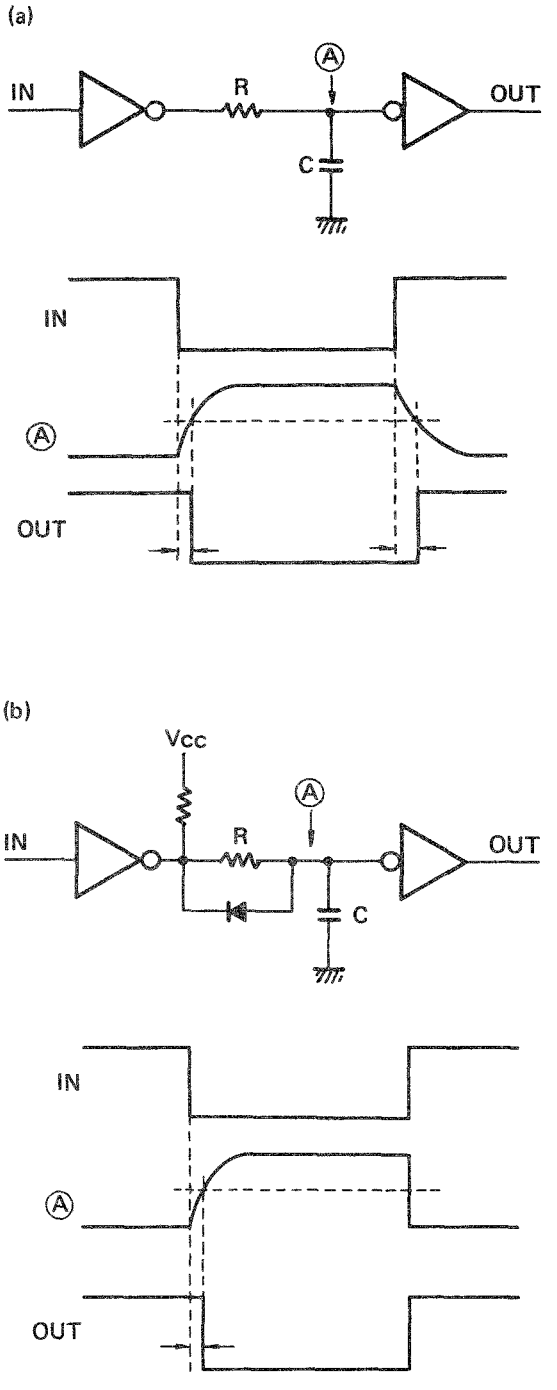


Fig. 30 Delay circuit

c) Trigger pulse generator

In Fig. 31, the inputs of the NAND gate do not coincide. However, this circuit outputs a negative trigger pulse for a short time while the NAND's inputs coincide with the help of the discharging current of C of the delay circuit.

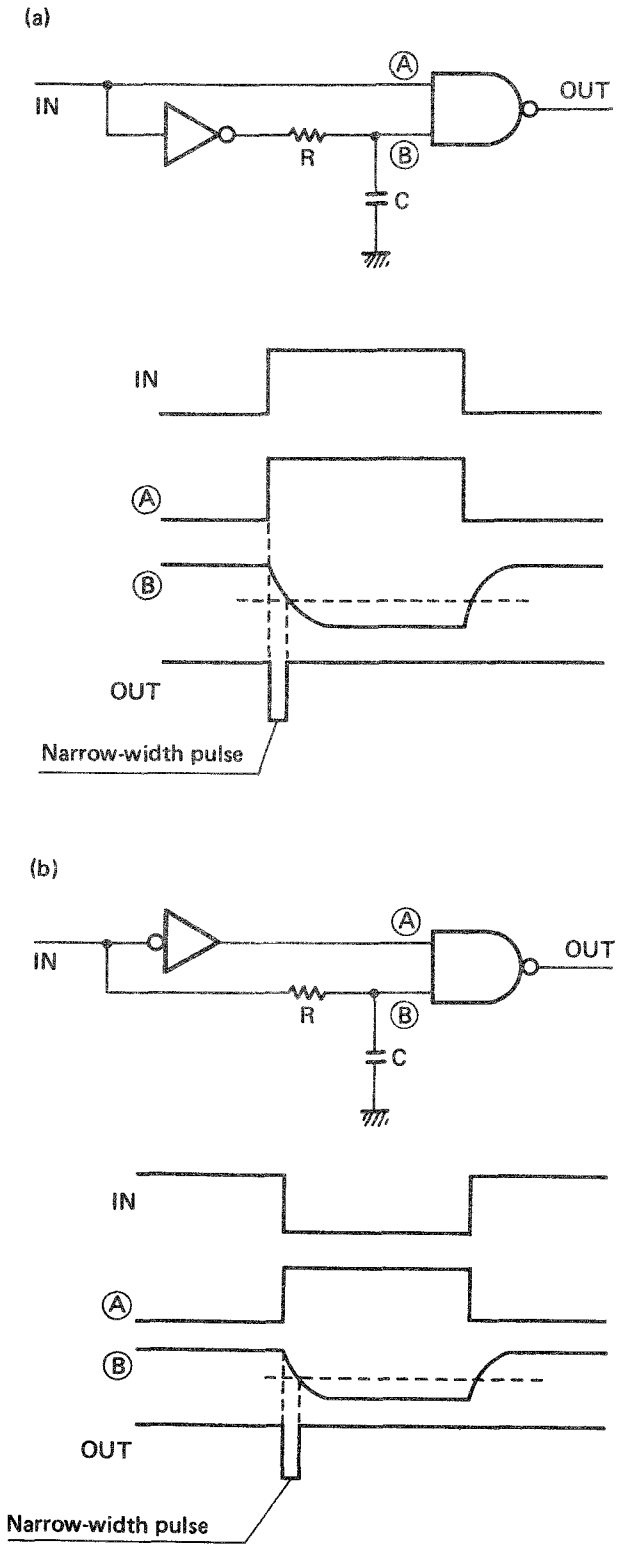


Fig. 31 Trigger pulse generator circuit

The circuit in Fig. 32 generates a positive pulse at the rising point of the square wave with two inverters.

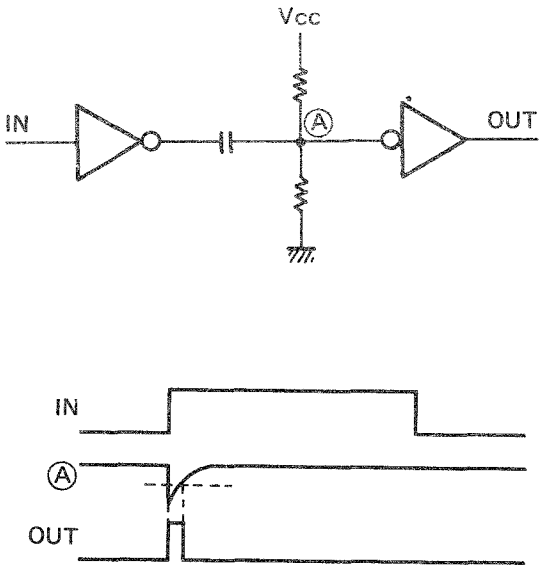


Fig. 32 Trigger pulse generator circuit

d) One-shot (monostable) multivibrator

A monostable multivibrator can be made using two NAND gates or two NOR gates along with capacitors and resistors. This circuit can be easily understood by expressing the first stage gate in OR logic. When the first stage is an Invert OR (NAND) gate, a negative output pulse can be obtained, and when it is a NOR gate, the output pulse is positive. The width of the output pulses will be determined by the time constant of C and R.

See Fig. 33.

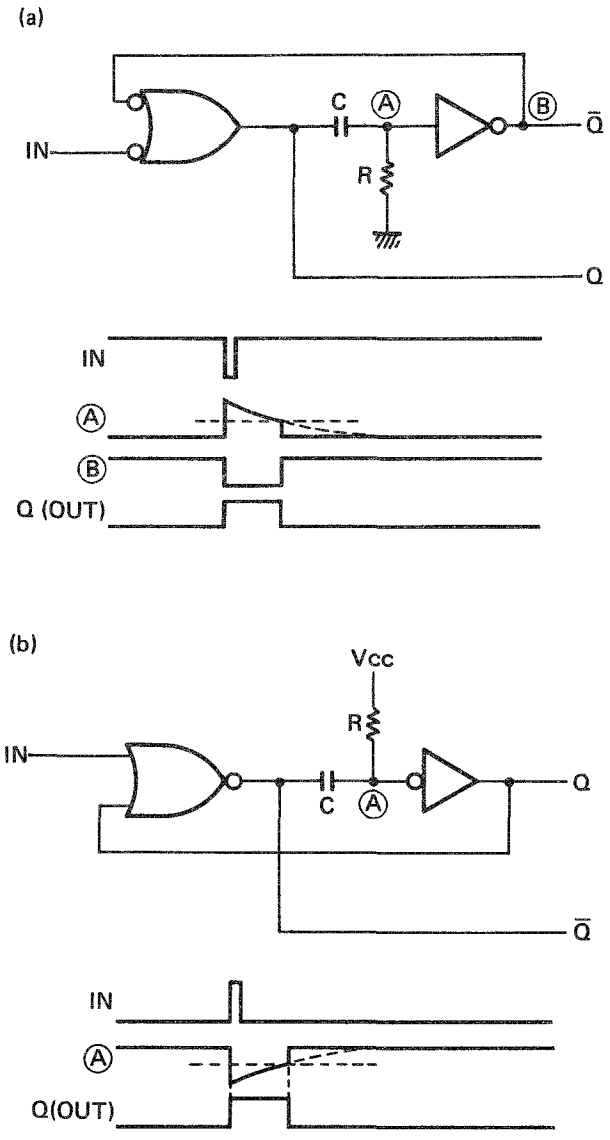


Fig. 33 Monostable multivibrator

e) Schmitt trigger circuit

The Schmitt trigger has a hysteresis input-output characteristic and is used for reshaping the input waveform into a square wave for use in the digital circuit. Hysteresis voltage width can be varied by adjusting Rs and Rf.

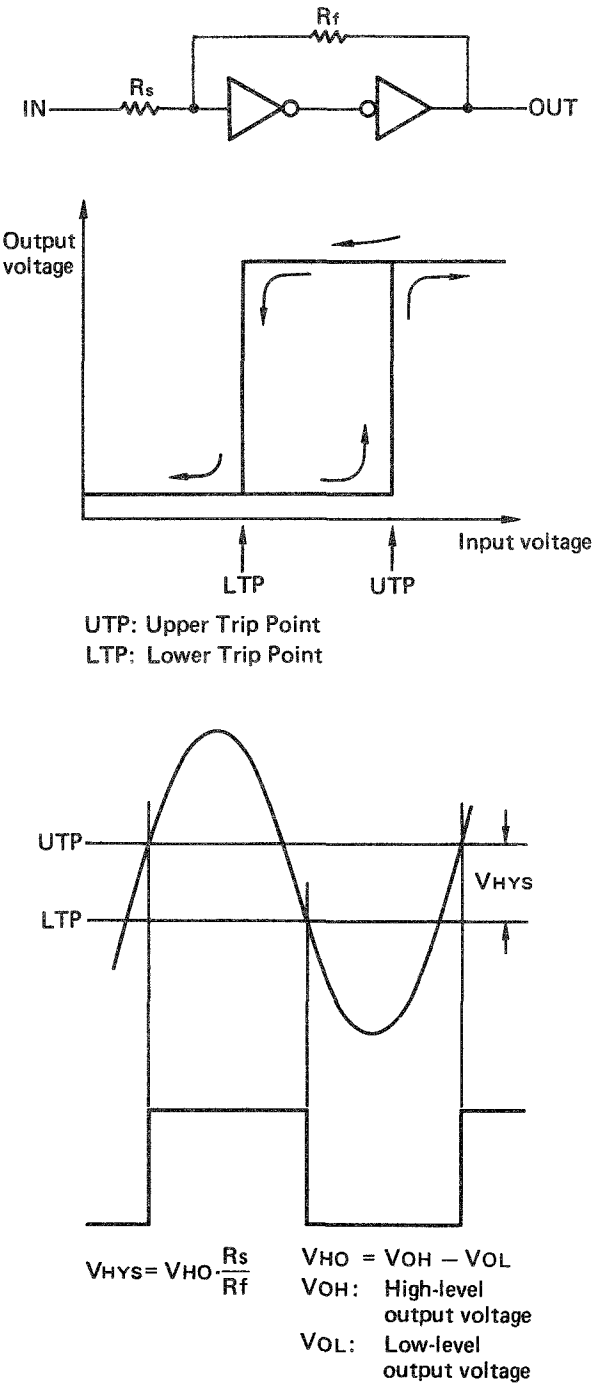


Fig. 34 Schmitt trigger circuit

f) Linear circuit

The input-output characteristic of an invert gate is nonlinear as shown in Fig. 35 (a). But, by adding a negative feedback resistor as in Fig. 35 (b), more linear characteristics can be achieved. In this way, it can be used as an analog amplifier circuit as well. The gain is expressed:

$$\frac{R_2}{R_1}$$

This circuit is used in an oscillator circuit which will be explained later.

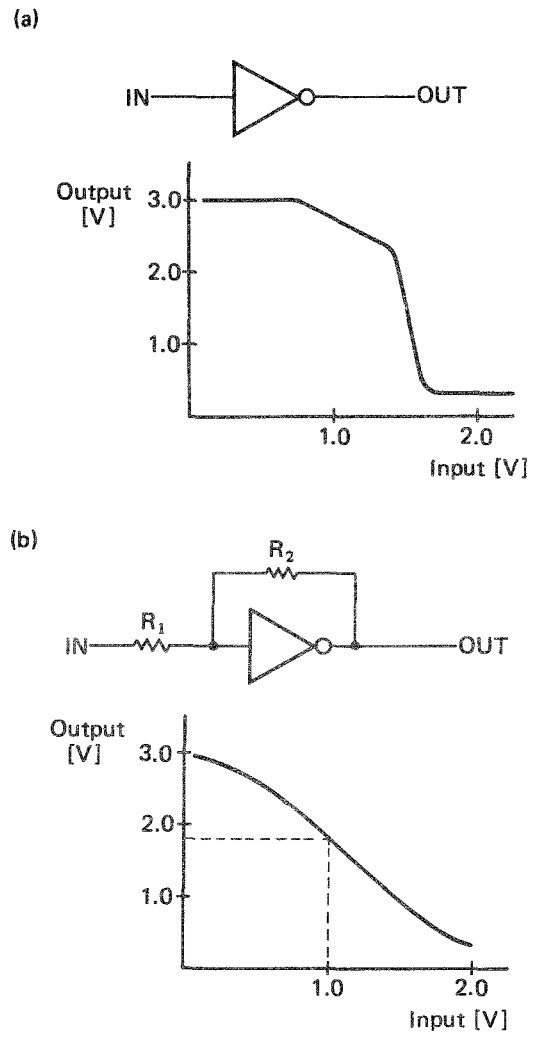


Fig. 35 Linear circuit

g) Astable multivibrator (Blocking oscillator)

Fig. 36 (a) shows a basic astable multivibrator circuit. A circuit which consists of two stages of linear circuits connected in series as illustrated in Fig. 36 (b). Since a capacitor appears in the feedback loop, the output frequency will be determined by the capacitance. This circuit is widely used in the design of a basic oscillator. Since the signal level exceeds the saturation point, rectangular waves appear at the output.

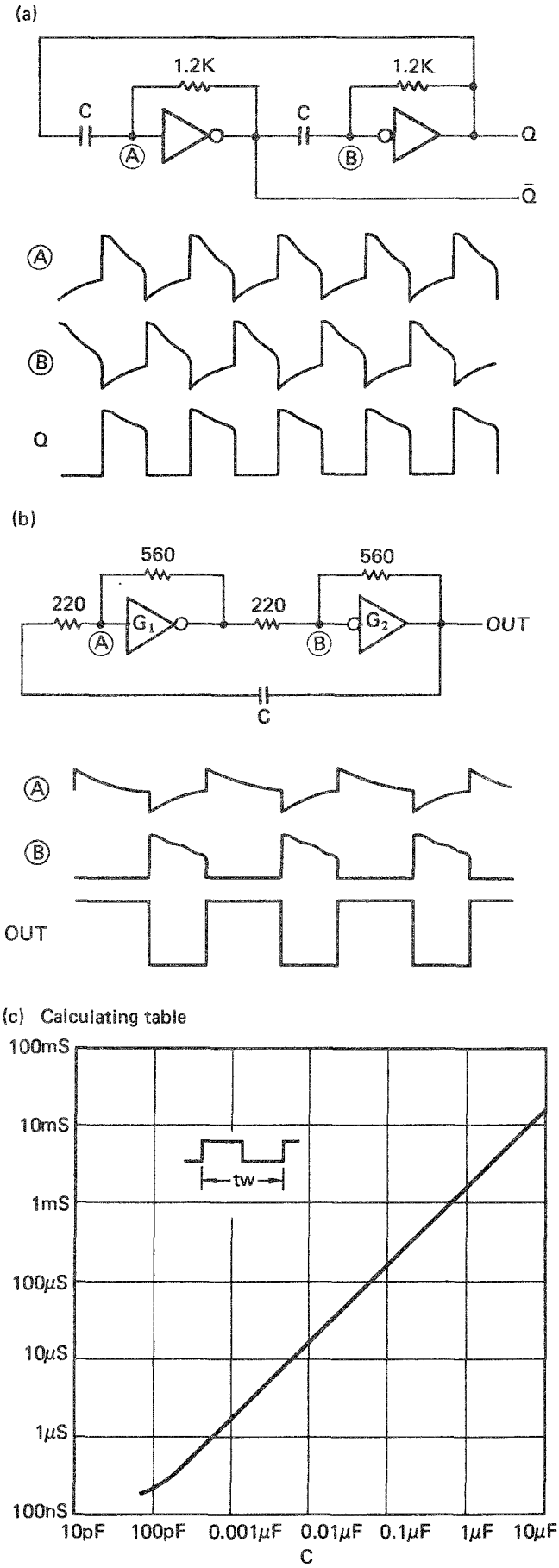


Fig. 36 Astable multivibrator

h) Quartz oscillator

The capacitor in the feedback stage of the astable multivibrator circuit in Fig. 36 (b) is replaced by a quartz oscillator. The wave form appearing at the output is close to a sine wave, as the oscillating level of the quartz is low—output does not reach saturation level. If a rectangular wave is required, connect a Schmitt trigger circuit shown in Fig. 34 to the output.

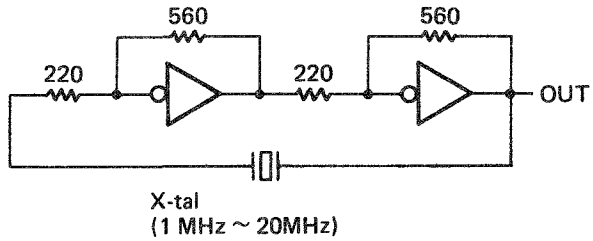


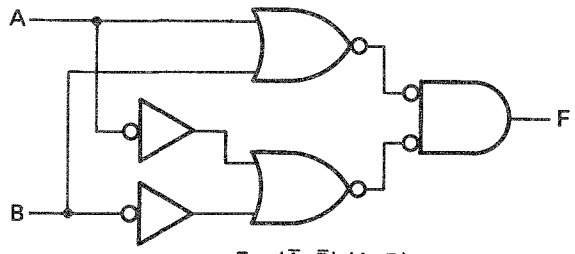
Fig. 37 Quartz Oscillator

i) Exclusive OR circuit

In this circuit, H (1) will appear at the output only when disagreeing signals are fed to the input terminals (A and B). This circuit can be made with invert gates. Fig. 38 (a) shows a circuit employing five NOR gates, while (b) illustrates a four NAND gate circuit (refer to Table 2). The symbol is shown in Fig. 38 (d).

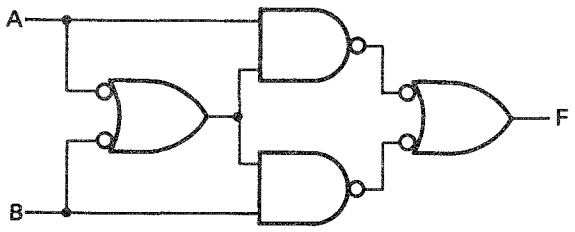
$F = A \oplus B$ stands for $A\bar{B}+\bar{A}B$. Therefore, $A \oplus B = A\bar{B}+\bar{A}B$.

(a)



$F = (\bar{A}+\bar{B})\cdot(A+B)$
$= A\bar{B} + \bar{A}B$

(b)



$F = (\bar{A}+\bar{B})\cdot A + (\bar{A}+\bar{B})\cdot B$
$= A\bar{B} + \bar{A}B$

(c) Truth table

A	B	F=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

(d) Symbol

Fig. 38 Exclusive OR circuit

5. Flip-flop

5-1. Sequential logic circuit

For the digital logic circuits and circuit combinations explained thus far, the only factor which influences signal transmission time is propagation time delay, the same as in the case of analog circuits, otherwise, whenever input is applied, output is obtained at once. However, this is not true with sequential logic circuits where output will not appear unless certain conditions are satisfied. Since the transmission takes time, the output is affected by signal sequence. Flip-flop circuits are typical of this type of logic circuit.

Time sharing is used for transmitting much information on a single channel as digital circuits have limited processing ability in a given time and have to operate signals in order. Their operation also necessitates external circuits. Sequential logic circuits answer such requirements. There are two types of sequential circuits: synchronous and asynchronous. Actually, combination and sequential circuits are used together, rather than separately.

Tense	Past	Present	Future
Digital Term	Tn-1	Tn	Tn+1

Table 5 Tense vs. digital term

This is very convenient in expressing circuit functions sequentially controlled by input signals.

5-2. Fundamental principle of flip-flop circuit

A flip-flop circuit is also called a "bistable multivibrator." The output of a combined circuit varies (L – H – L or H – L – H) in accordance with the variation of its input (L – H – L). By the same input variation, the output of a flip-flop sequential circuit may be shifted from L to H during the time from Tn-1 to Tn. But the H level may be kept unchanged during the time from Tn to Tn+1. This means that the circuit has a memory function for holding the output level from Tn to Tn+1. The output variation of a sequential circuit depends on its composition and the time factor as there are various kinds in the circuits available.

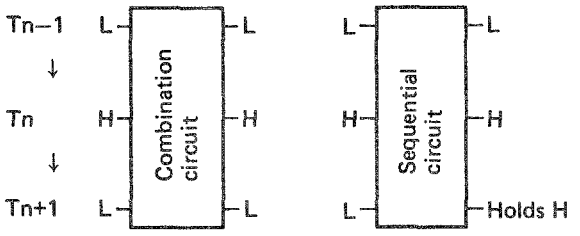


Fig. 39 Combination and sequential circuit output variations based on input

Flip-flop circuits are classified into four types by function:

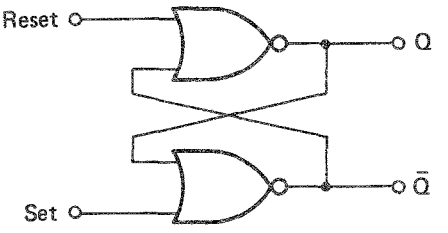
One-bit memory circuit
One-clock pulse delay circuit
Binary counter circuit
1/2 frequency divider

5-3. Flip-flops classified by logical function

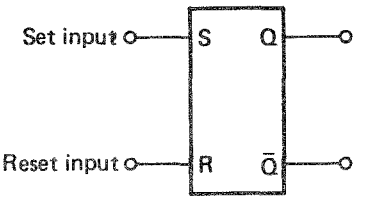
a) R-S latch

The fundamental sequential logic circuit has two invert gates which are crosscoupled as shown in Fig. 40. A latch is a feedback loop used in a symmetrical digital circuit (such as a flip-flop circuit) to retain a state. It has two input terminals of SET and RESET and has two complementary outputs of Q and $\overline{Q}$. The function table for a NOR gate R-S latch is shown in Fig. 40 (c). It is important not to make both the R and S input levels High (1) and then Low (0) simultaneously. As shown in Fig. 40 (c), the outputs do not complement each other when both R-S inputs are H (1). When both R and S inputs shift to L (0), the output levels become indeterminate, although Q and $\overline{Q}$ are complementary.

(a) Logic circuit



(b) Symbol



(c) Function table

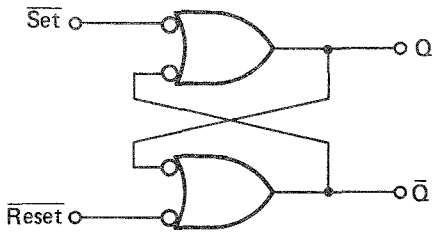
Input		Output	
S	R	Q	$\overline{Q}$
L	L	Unchanged	
L	H	L	H
H	L	H	L
H	H	*	*

*: Q = $\overline{Q}$ = L: Inhibition

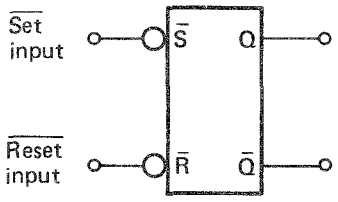
Fig. 40 NOR gate R-S latch

Although Fig. 40 consists of NOR gates, an R-S latch can be made of NAND gates, and expressed by Invert OR circuit as shown in Fig. 41. The R-S latch itself is used as a temporary memory circuit. This is widely applied to complicated flip-flop circuits in combination with control gates and other latches.

(a) Logic circuit



(b) Symbol



(c) Function table

Input		Output	
S̄	R̄	Q	Q̄
H	H	Unchanged	
H	L	L	H
L	H	H	L
L	L	*	*

* Q = Q̄ = H: Inhibition

(d) Timing chart

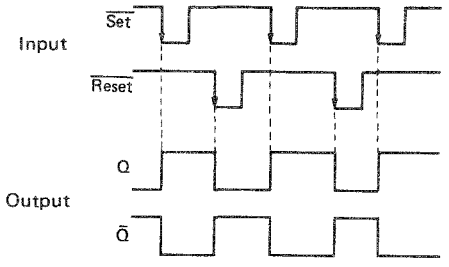


Fig. 41 NAND gate R-S latch

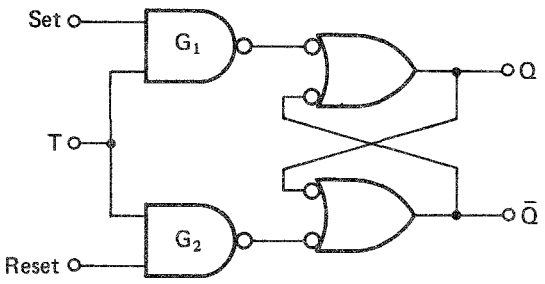
b) R-S-T flip-flop (FF)

The Q and Q̄ outputs of an R-S latch vary quickly in accordance with the variation of R-S inputs. When synchronous variation is required to clock signals, a synchronous FF like that shown in Fig. 42 (a), simple R-S-T FF, is employed. This is a double-phase circuit consisting of four NAND gates. Two gates compose an R-S latch. Two other gates, G_1 and G_2 are added to the circuit to synchronize R and S inputs with T. Fig. 42 (c) and (d) show the R-S-T FF's function table and timing chart. When no clock signal is present at T, the outputs of G_1 and G_2 become L and the R-S latch retains its state. When a clock signal appears, R-S inputs are inverted by G_1 and G_2 and then fed to the R-S latch.

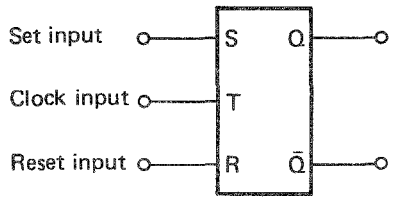
With the FF in Fig. 42, Q and Q̄ vary many times with the quick variation of R-S inputs during the period when a clock signal is present.

The synchronous type only changes its output state once with each clock signal. To realize this, it is necessary to narrow down the width of the clock signal. This will be explained later.

(a) Logic circuit of 2-phase type R-S-T FF



(b) Symbol



(c) Function table

Tn		Tn+1	
S	R	Qn+1	Q̄n+1
L	L	Qn	Q̄n
L	H	L	H
H	L	H	L
H	H	*	*

Tn: Bit time before clocked
Tn+1: Bit time after clocked
Qn: Retains the state before clock inputs
* : Qn+1 = Q̄n+1 = H: Inhibition

(d) Timing chart

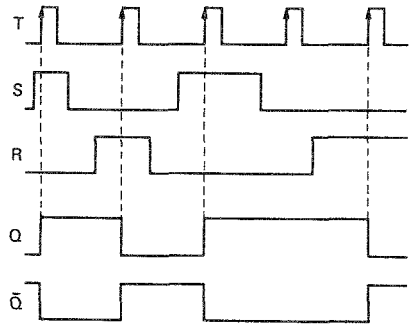


Fig. 42 R-S-T flip-flop

c) JK flip-flop

As shown in Fig. 43, a JK FF is also synchronous and has JK inputs instead of R-S inputs like the R-S-T FF. As shown in Fig. 43 (c), the JK flip-flop accepts any input combination. Feeding H to both inputs of an R-S-T FF simultaneously is inhibited, but it is all right with a JK FF because it only inverts the output state of the time before the clock signal is applied.

As shown in Fig. 44, JK FF is basically an R-S-T FF which has been made stable and changes its output state only once with each clock signal. In the JK FF, J input and $\bar{Q}$ output are fed to SET input, and K input and Q output to RESET input. Thus there is no R:S = H:H input combination for an R-S-T FF.

It should be noted that the circuit may oscillate if the clock signal pulse width is wide.

(d) Timing chart

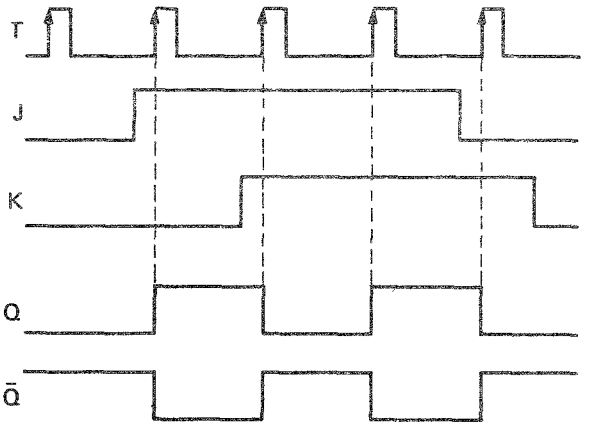
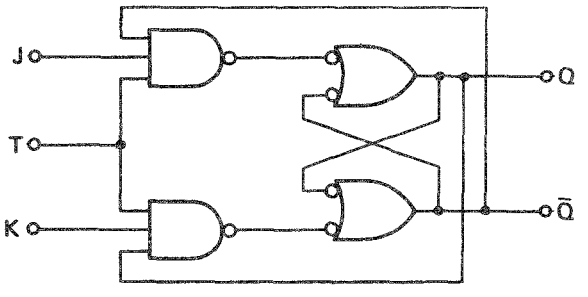


Fig. 43 JK flip-flop

(a) Logic circuit



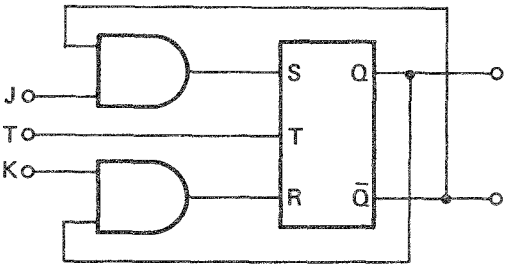
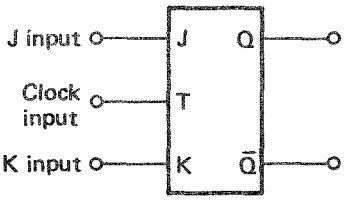


Fig. 44 JK FF consisting of R-S-T FF

(b) Symbol



(c) Function table

Tn		Tn+1
J	K	Qn+1
L	L	Qn
L	H	L
H	L	H
H	H	$\bar{Q}$n

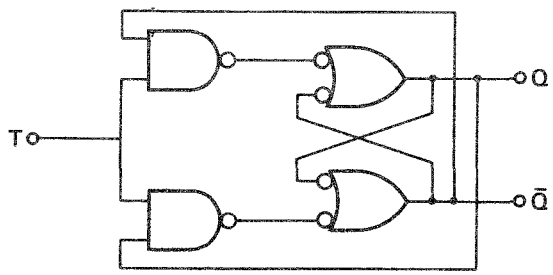
Qn: Retains the state before clock inputs

$\bar{Q}$n: Inverts the state before clock inputs

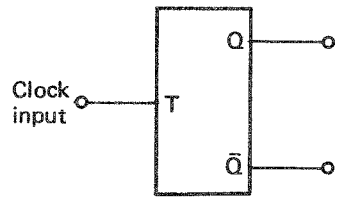
d) T flip-flop

With a T FF, the Q and $\overline{Q}$ outputs change while a clock pulse is present. Therefore, clock pulse width should be narrow as wide pulses cause chattering or frequent switching. The reason and method will be explained in 5-4.

(a) Logic circuit



(b) Symbol



(c) Timing chart

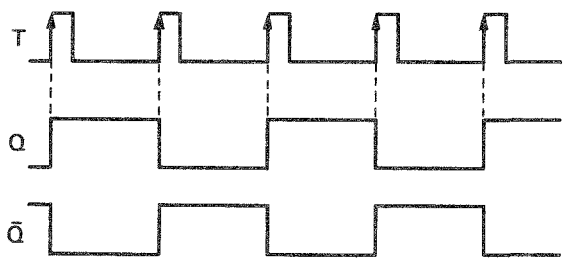
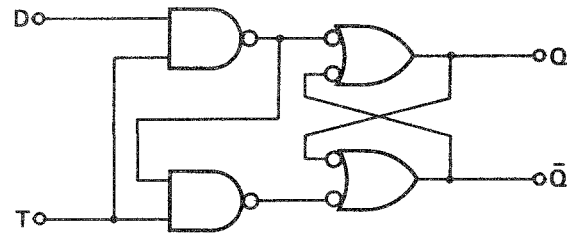


Fig. 45 T flip-flop

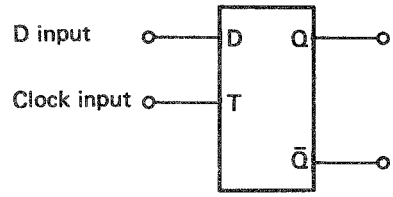
e) D (Delay) flip-flop

As shown in Fig. 46, a D FF has a data input, a clock input and Q and $\overline{Q}$ outputs. When both D and T are H, Q becomes H and $\overline{Q}$ becomes L, and when D is L and T is H, Q becomes L and $\overline{Q}$ becomes H. Thus, signals applied to D appear at the output every time a clock signal is applied.

(a) Logic circuit



(b) Symbol



(c) Function table

Tn	Tn+1
D	Qn+1
L	L
H	H

(d) Timing chart

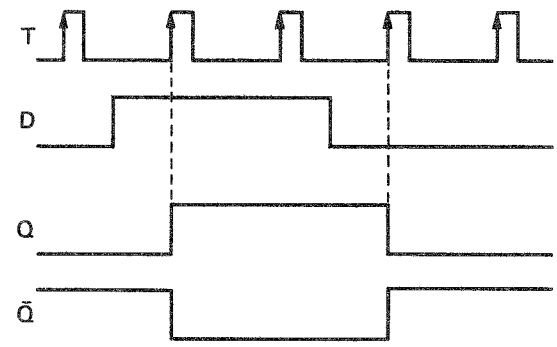


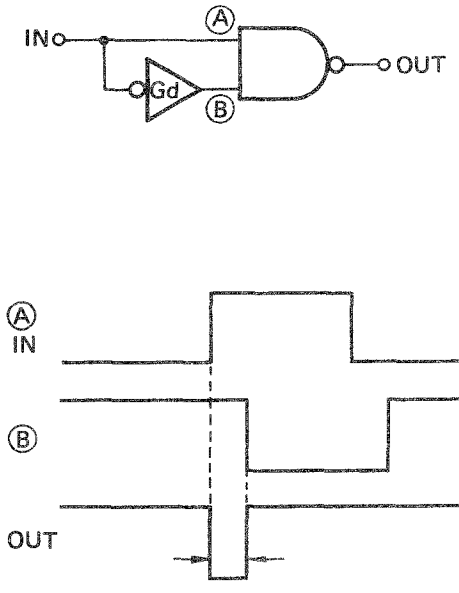
Fig. 46 D flip-flop

5-4. FF's classified by trigger system

As mentioned before, the outputs of a T FF change their state many times during the presence of a clock signal, thus T FF's are liable to oscillate.

a) Edge trigger system

To overcome the oscillation problem, the edge-trigger—very narrow width pulse—system has been developed. This system narrows the clock pulse-width, reads the input and kills the clock signal immediately after the outputs are changed. In narrowing the clock pulse-width, picking out clock-pulse edges using the gate's propagation delay time is popular, although a different method is used with CR differential circuits.



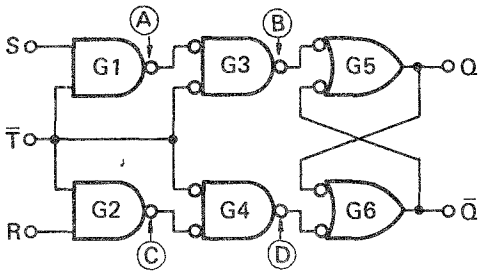
Pulse width depends on Gd's delay time.

Fig. 47 Edge detection circuit

Gates corresponding to the Gd of Fig. 47 are G1 and G2. The circuit shown in Fig. 48 changes its outputs at the falling, or negative, edge of clock pulses.

Fig. 48 shows an R-S-T FF employing the edge-trigger system.

(a) Logic circuit



(b) Timing chart

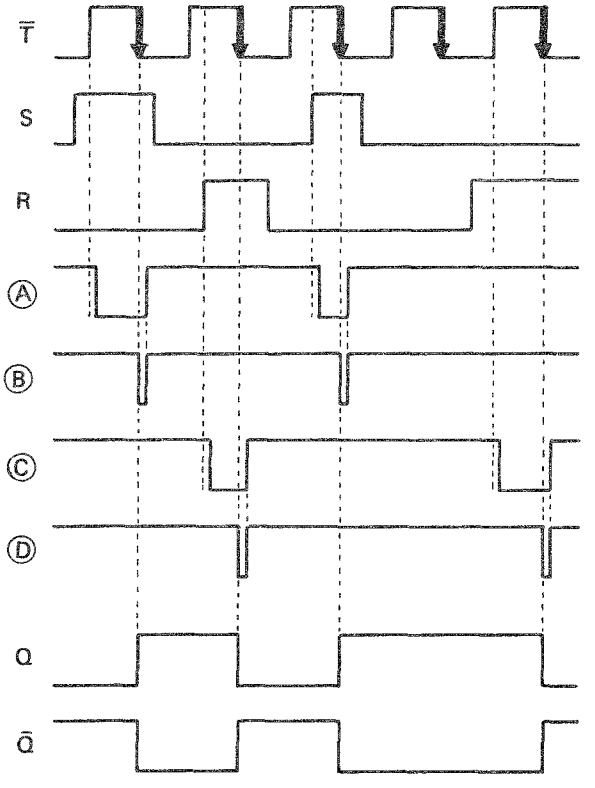


Fig. 48 Edge-trigger R-S-T FF

b) Master-slave system

The master-slave system prevents misoperation by varying outputs when the clock signal disappears, while the edge-trigger system prevents frequent output variation by narrowing pulse signal width. This system has two sets of R-S-T FF's which are a master FF and slave FF as shown in Fig. 49. An inverted clock signal is fed to the second FF. When the clock signal is L, L is applied to the input of G1 and G2, and q and $\overline{q}$ remain unchanged. At this time, an inverted clock signal H is fed to G3 and G4. The states of q and $\overline{q}$ are then fed into the slave FF whose signals appear at Q and $\overline{Q}$. When the clock signal becomes H, the master FF reads the states of S and R, and outputs q and $\overline{q}$. However, Q and $\overline{Q}$ remain unchanged because G3 and G4 close. When the clock signal changes to L again, the slave FF reads the states of q and $\overline{q}$ and outputs signals at Q and $\overline{Q}$. This means that the outputs vary when the clock signal falls from H to L. Most of the FF IC's on the market are either master-slave or edge-trigger type. The clock input of each can be classified into two types as shown in Table 6.

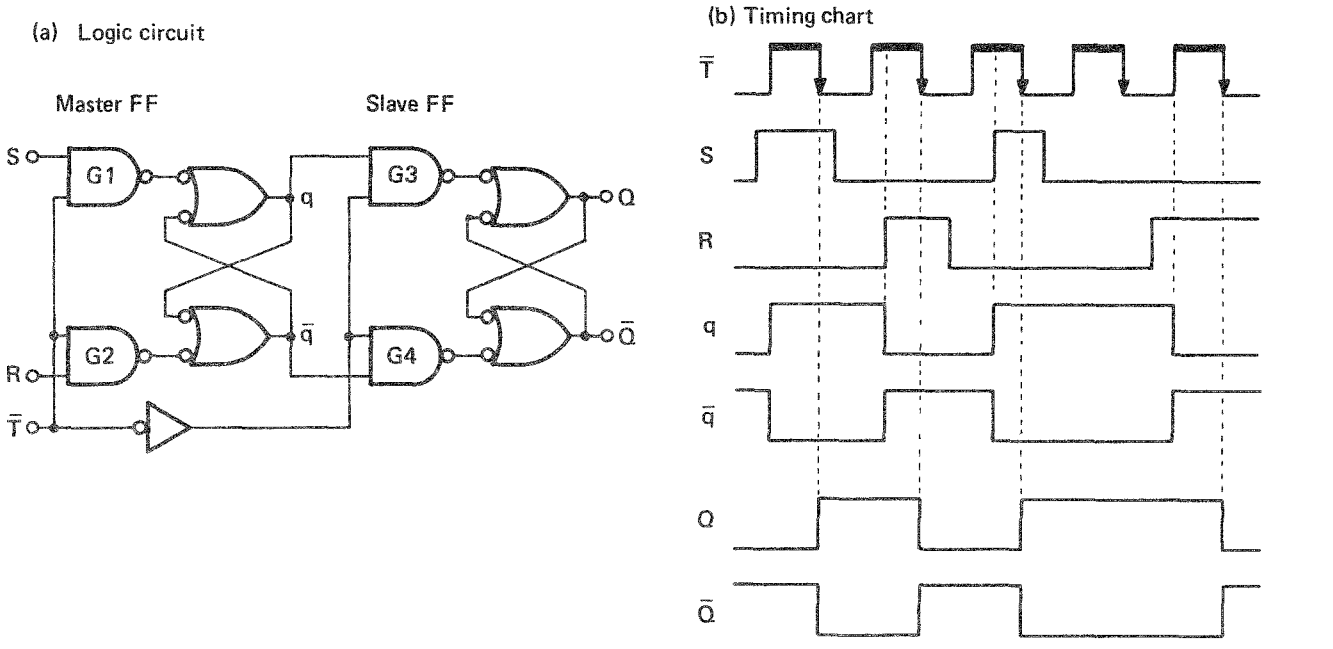


Fig. 49 Master-slave type R-S-T FF

Type		Logic symbol	Position of clock input where output shifts	Function of the FF
Master-slave system	Positive going trigger	T		It reads input signal while clock level is L. Output shifts in accordance with function table when clock shifts to H.
	Negative going trigger	$\overline{T}$		It reads input while clock level is H. Output shifts in accordance with function table when clock shifts to L.
Edge trigger system	Positive going trigger	T		It reads input when clock level shifts to H. Output shifts in accordance with function table at the same time.
	Negative going trigger	$\overline{T}$		It reads input when clock level shifts to L. Output shifts in accordance with function table at the same time.

Table 6 Trigger systems

6. Binary system

6-1. Decimal and binary

To transmit and process data digitally, it is necessary to change it into a form that can be processed by electronic circuits as shown in Fig. 50.

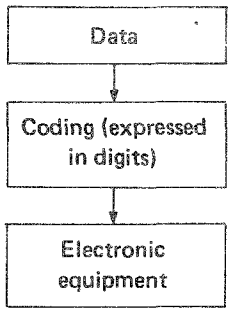


Fig. 50

The most appropriate way of handling a large amount of information or data is numerically. Of course, a fixed coding system is required to change one form into another. If we try to introduce decimalization as used in everyday life, we have to divide the limited voltage range into small parts as shown in Fig. 51. This requires ten transfer lines.

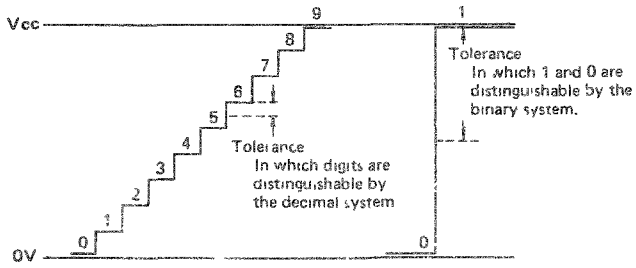


Fig. 51

Such voltage range division decreases error allowance, and it is not wise to increase the number of transfer lines. A decimal number with the smallest digit called LSD (Least Significant Digit) and the largest, MSD (Most Significant Digit) is weighted by 10, 100, 1,028 and so on.

On the other hand, as digits 0 and 1 are used to express any number in the binary system, a carry is made with every odd number. Unlike the everyday decimal system, numbers are expressed in bits (binary digit). As shown in Fig. 53, each of the four bits has a weighting of 2^0, 2^1, 2^2 and 2^3, in that order from the smallest bit.

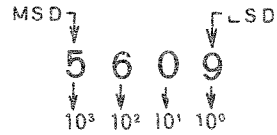


Fig. 52 Weighting of decimal numbers

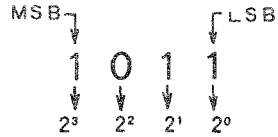


Fig. 53 Weighting of every bit in the binary system

Table 7 shows the binary equivalents of decimal numbers. Such equivalents are easily obtained when the digits are small, but difficult when they are big. It is useful, therefore, to remember the conversion system for big-digit numbers.

Decimal	Binary
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111
•	•
•	•
•	•

Table 7 Binary equivalents of decimal numbers

6-2. Decimal/binary and binary/decimal conversion

To convert a decimal number to a binary number, the former should be divided by two to the nearest whole digit, as shown in Fig. 54. When the number is divisible, write 0; when it is indivisible and 1 is left, place 1 to the right of the quotient. Then divide the quotient by two again and record a new quotient and residual, until the quotient becomes 0. The residuals obtained represent the binary equivalent of the original decimal number. The first residual (0 is also a residual) is the LSB and the last is the MSB.

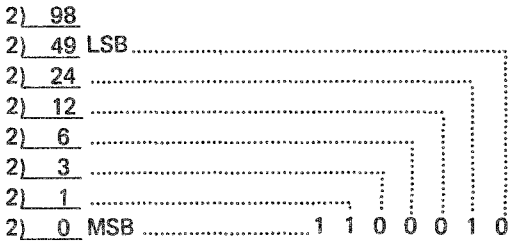


Fig. 54 Decimal/binary conversion

As every binary number is weighted as shown in Fig. 53, it can be converted into a decimal number by multiplying each bit's weighting by its value. This is shown in Fig. 55.

$1100010_{(2)}$
$= 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$
$= 98_{10}$

Fig. 55 Binary/decimal conversion

When there are many figures, this method may prove troublesome. In such a case, convert by calculating in groups of four figures each. It is easy to obtain equivalents of four-bit binary numbers as shown in Fig. 56.

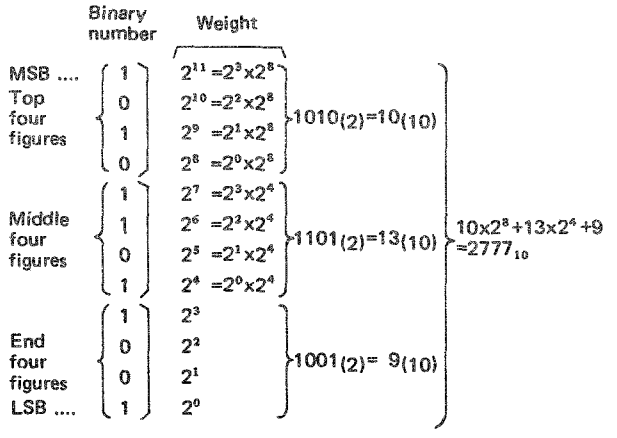


Fig. 56 Binary/decimal conversion

Divide weighting into two stages to obtain four-bit numbers and then convert them into decimal numbers. In the example shown in Fig. 56, multiplying the top four bits by a weighting of 2^8, and the middle four bits by a weighting of 2^4 produces the decimal equivalent.

6-3. Binary coded decimal (BCD)

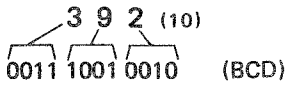
BCD is a code system frequently used for the binary expression of decimal numbers by 1 and 0. Under the system, numbers from 0 to 9 are expressed in four-bit binary numbers as shown in Table 8 (same as ordinary binary equivalents of decimal numbers), and every decimal number is expressed by a four-bit binary number. Binary four-bit numbers can actually represent up to 15 of the decimal system, but combinations for 10 to 15 are not used under the BCD coding system.

Decimal	BCD				
	8	4	2	1	
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
•	1	0	1	0	Not used under the BCD system
•	1	0	1	1	
•	1	1	0	0	
•	1	1	0	1	
•	1	1	1	0	
•	1	1	1	1	

Table 8 Decimal number/BCD code

Every bit of a four-bit binary number representing a decimal number has a weighting of 8,4,2 and 1 just like a binary code. In this context, the BCD code system is sometimes called the 8421 code system. Now let's see how the decimal number 392 is expressed in BCD code. The appropriate code can be obtained by writing four-bit binary numbers for each 3, 9 and 2 as shown in Fig. 57 (a). The entire code will thus have 12 bits. For comparison, Fig. 57 (b) shows the conventional binary representation of 392. The binary code, having only nine bits, is quite different from the BCD code.

a) BCD code



b) Conventional binary code

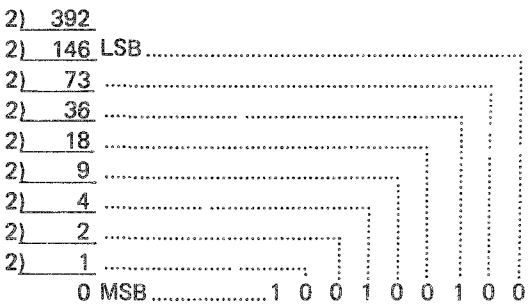


Fig. 57 Difference between BCD and conventional binary codes

This may give you the impression that the conventional binary code is better and simpler, having less bits. But the reverse is the case. In expressing large decimal numbers by binary codes, the number of bits will increase endlessly, making it very difficult to design a circuit. Although the number of bits for the entire BCD code will also increase, since each decimal digit can be expressed in four bits, a BCD code can be obtained as bit-parallel serial data by using only 10 switches, four transmission lines and several gates, as shown in Fig. 58.

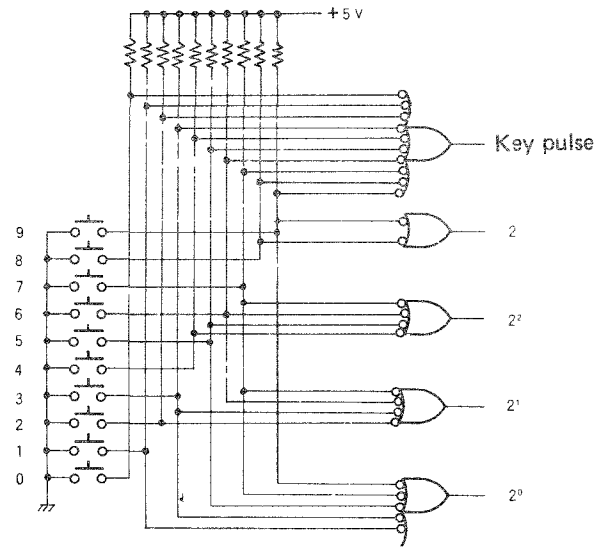


Fig. 58 Decimal-BCD encoder (bit-parallel serial data)

In electric typewriters and electronic calculators, BCD code conversion and operation is carried out by pressing a key switch. An increasing number of measuring instruments, including frequency counters and wow/flutter meters, now have BCD outputs for printers. Other binary coding systems include excess-three code and Gray code systems. However, since these are not generally used, we won't discuss them here.

7. Counter

7-1. Asynchronous binary counter

Most digital circuits except AND and OR gates are used as counters, and the asynchronous binary type is the simplest. JK FF or D FF can be wired as shown in Fig. 59 and used in the so-called toggle mode by inverting outputs when the clock pulse falls.

Let us look at the relation between the input clock pulse (CK) and output (Q). If Q was "0" originally, it inverts to "1" when the first pulse falls, and to "0" when the second pulse falls. In the same way it repeats the inversion every time the CK falls. Fig. 59 shows a negative type edge-trigger flip-flop. The positive type works the same as the negative type except that Q inverts when CK rises. These circuits work as 1/2 frequency dividers. You will see in Fig. 60 that they also work as binary counters shifting their outputs to "0" whenever an even number pulse falls and to "1" whenever an odd number pulse falls.

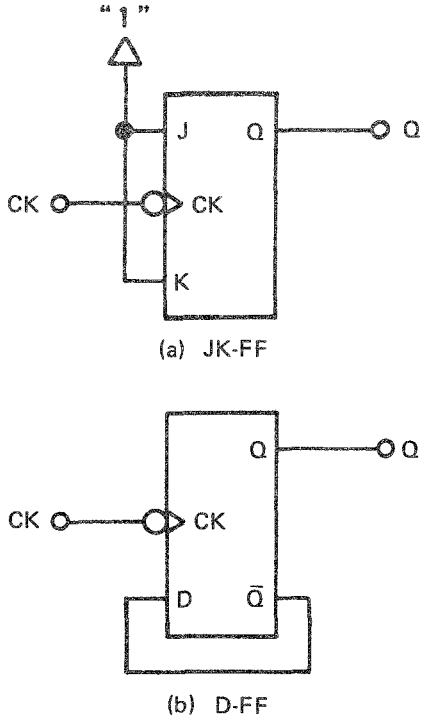


Fig. 59 FF binary counter

What happens then when the circuits are connected in series as in Fig. 61? The whole circuit becomes a 1/8 frequency divider. If outputs $Q_0 \sim Q_2$ were 0 originally and were considered to be a three-figure binary number, then the whole circuit would become an octal counter. By connecting units of flip-flops in series, a 2^n-radix (base) counter can be made.

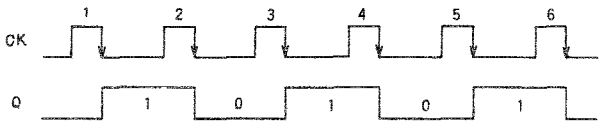


Fig. 60 Timing chart of binary counter

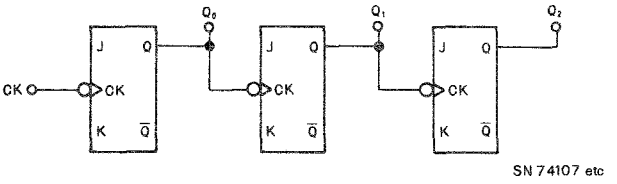


Fig. 61 Asynchronous octal Up counter

7-2. Up/Down counter

The coded number of the Up counter in Table 9, taken from the Q outputs, increases when clock pulses are fed into the counter (increment). The timing chart of each FF output is shown in Figs. 62 and 63. Conversly, the number of a Down counter taken from $\bar{Q}$ decreases as pulses are fed (decrement). A Down counter is useful for making a circuit which shifts the function of a device when it has finished counting specified pulses. The octal Up counter in Fig. 62 can be modified to a Down counter by taking the output from $\bar{Q}$ instead of Q in all cases.

Output of octal counter

T	Q_2	Q_1	Q_0	decimal
T_0	0	0	0	0
T_1	0	0	1	1
T_2	0	1	0	2
T_3	0	1	1	3
T_4	1	0	0	4
T_5	1	0	1	5
T_6	1	1	0	6
T_7	1	1	1	7
T_8	0	0	0	0
T_9	0	0	1	1
•				
•				
•				

Table 9 Table of octal counter (T: number of pulses)

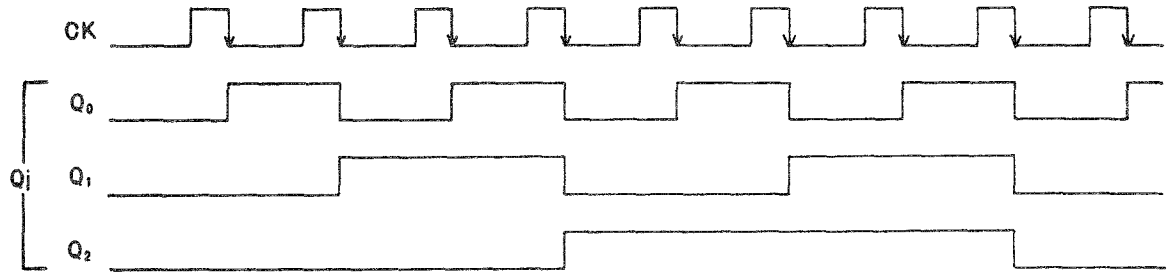


Fig. 62 Octal Up counter timing chart

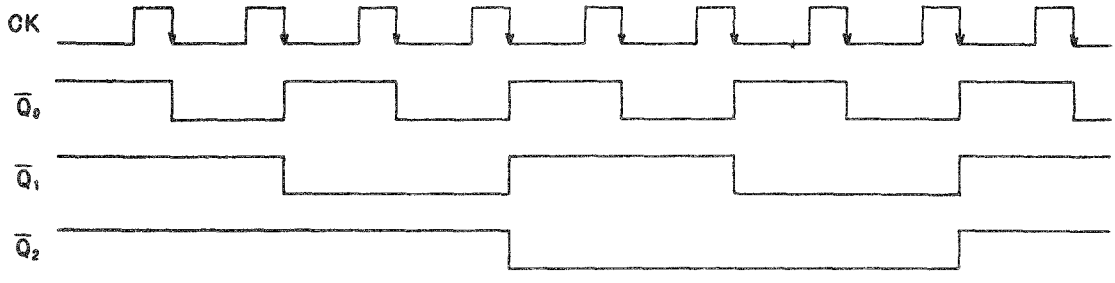


Fig. 63 Octal Down counter timing chart

7-3. N-radix system

What about making decimal and duo-decimal counters? A simple method is to count up from 1 to 10, sense it, and then clear all flip-flops. Fig. 64 shows a decimal counter. The binary code expression of decimal 10 is "1010". A four-input NAND gate senses the number "1010" and clears all flip-flops. To make a N-radix counter, N units of flip-flops which satisfy the following formula are required.

$$2^{n-1} < N \leq 2^n$$

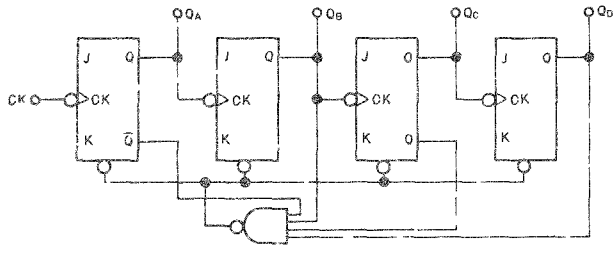


Fig. 64 Asynchronous decimal counter

Fig. 65 shows a TTL-MSI decimal counter. The circuit can use a manipulate method as a binary-quinary or a quinary-binary counter and has terminals for resetting to 0 or 9.

When using this circuit as a binary-quinary counter, its output becomes BCD.

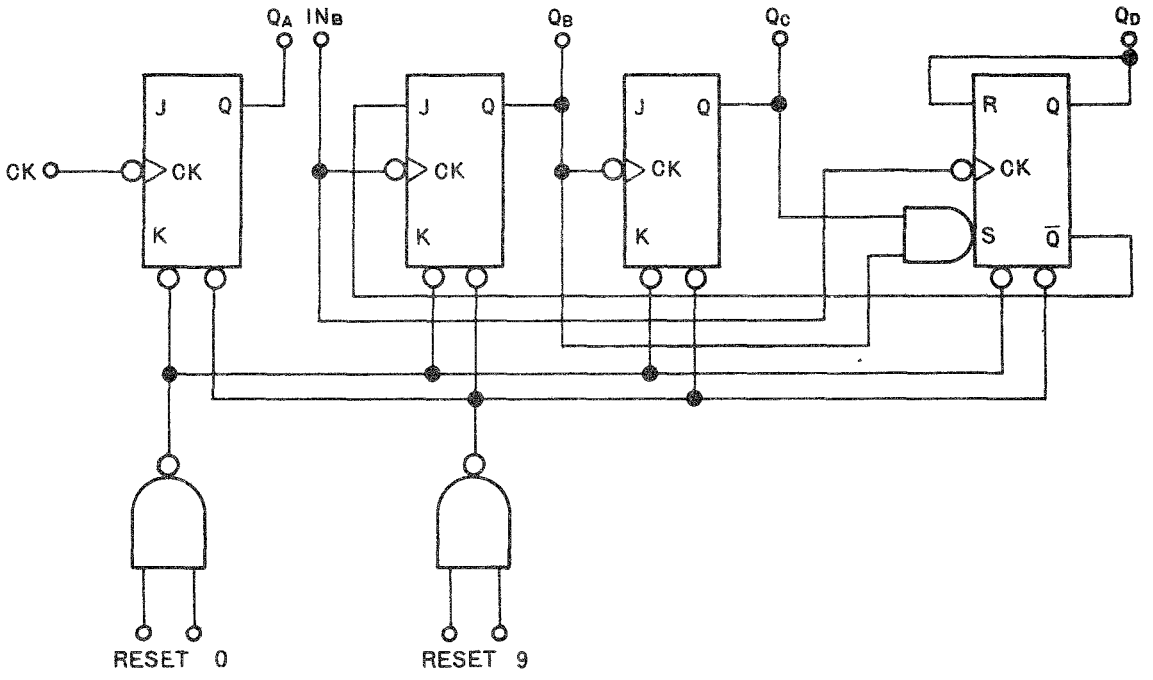


Fig. 65 MSI decimal counter SN7490

7-4. Synchronous counter

All the counters explained so far are asynchronous type (Ripple counter). Time lag between input and output signals are inherent to the flip-flop used. A TTL's time lag is 10–30ns. The more stages, the longer the delay becomes. This presents a problem when using the counter as a timing device and connecting more than two outputs except when using it as a frequency divider. As shown in Fig. 67, even an octal counter gives undesirable output codes such as 011 → 010 → 000 → 100 during the time that CK is fed to the input until the output stabilizes. The incorrect output causes the trigger circuits to malfunction. To prevent this, it is necessary to make the CK level of every flip-flop invert at the same time.

A synchronous counter solves the problem. These vary in composition. The principle, however, is the same as that of asynchronous counters. The output of the counter is inverted when the outputs of all preceding flip-flops are 1. Synchronous counters are more complicated than asynchronous ones. Fig. 68 shows a synchronous type octal counter. You will notice that all flip-flops are controlled by the same clock pulse synchronoulsy.

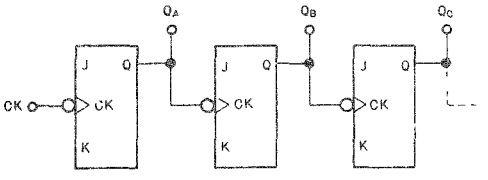


Fig. 66 Asynchronous counter propagation delay

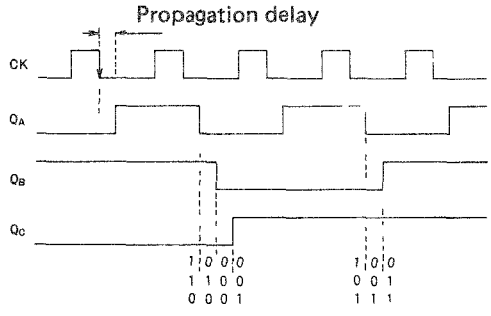


Fig. 67 Timing chart of asynchronous counter

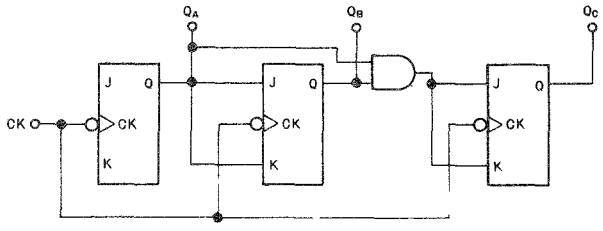


Fig. 68 Synchronous octal counter

7-5. MSI counter

Usually, separate flip-flops are not used for counters since MSI's (Middle Scale Integration) have become readily available. Figs. 69 and 70 show an MSI counter. This is a synchronous type and is capable of both count-up and count-down functions. This is a 4-bit (a 4 flip-flop) counter and is capable of binary-hexadecimal counting by using asynchronous Clear (which makes all flip-flops "0") and Load (which gives flip-flops original values) for carry, borrow and clear. Further, counting more than 16 is possible by connecting carry (borrow) to count up (count down). But, it should be noted that each MSI works asynchronously in this case.

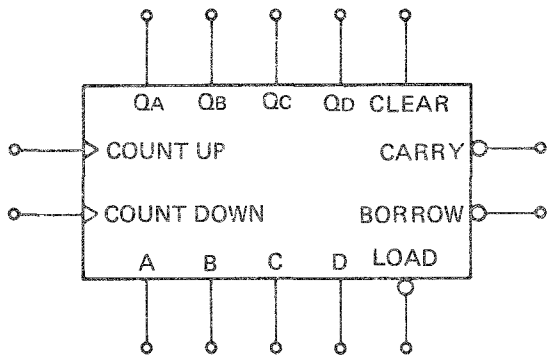
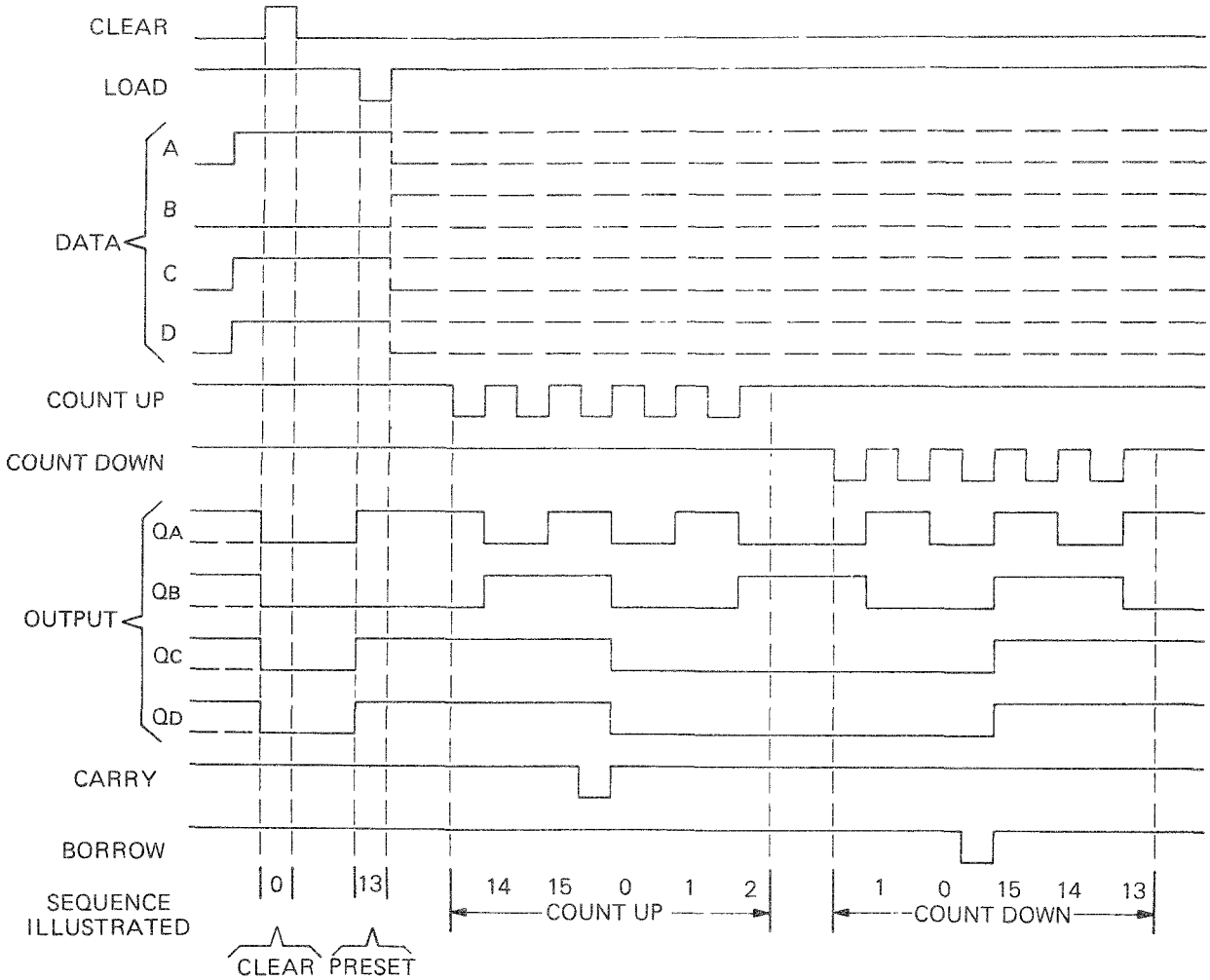


Fig. 69 MSI 4 bits counter SN74193

7-6. Decoder circuit

The output codes of counters or signal lines are mostly binary or similar to binary. Decoding binary values is necessary as it is hard to read them. Decoder IC's are available, although you can design a decoder by yourself by combining a number of gates. The indicator in Fig. 71 lights an LED which corresponds to the input code. The block diagram of an SN7445 is shown in Fig. 72, while its function table appears in Table 10.



NOTES. A. Clear overrides load, date, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Fig. 70 Timing chart of SN74193

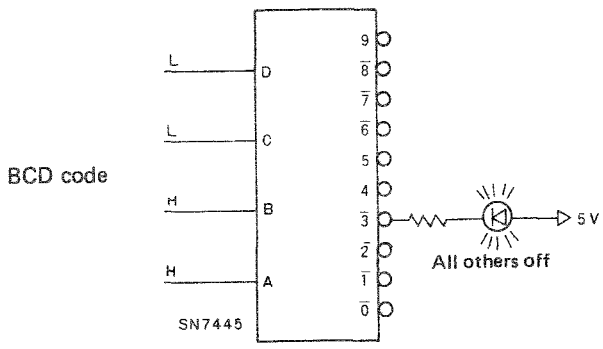


Fig. 71 BCD-decimal decoder and LED indicator

NO.	Input				Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (OFF). L = low level (ON)

Table 10 Function table of SN7445

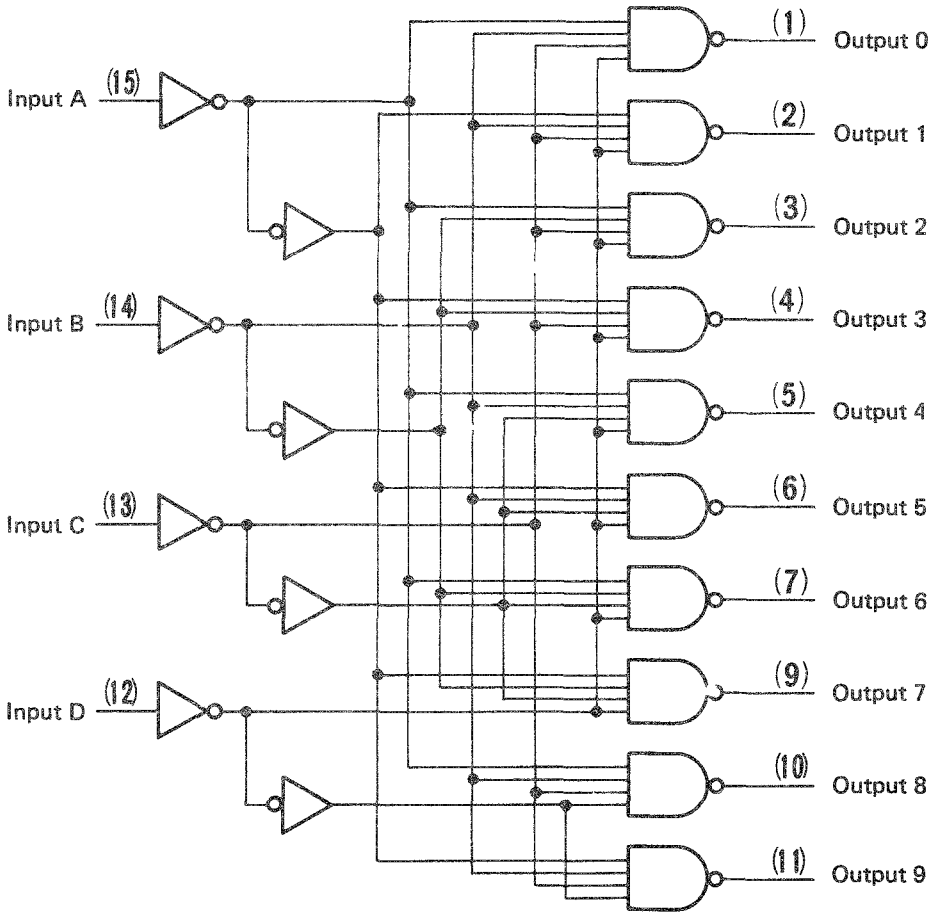


Fig. 72 Functional block diagram for SN7445

A 7-segment decoder turns LED's on and off to form figures as shown in Fig. 73. IC's SN7446 ~ 49 have this function. Some decoders have an ENABLE input as shown in Fig. 74 which allows all outputs to be turned off. The decoder is sometimes called a Data Demultiplexer because of its switching function which conveys ENABLE input to a specified output terminal.

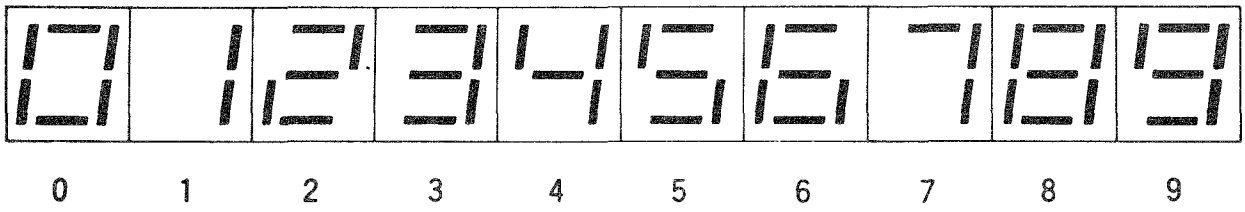


Fig. 73 7-Segment LED

7-7. Counter circuit application (clock)

The counter circuit is popularly applied to digital clocks, which work by counting pulses of a reference frequency. If the line frequency is 60Hz, one second can be recognized by counting 60 peaks of the alternating current, one minute by counting 60 seconds, and so on. Time indication can be done with 7-segment LED's and an exclusive decoder. What about time setting? Most of the digital clocks on the market go fast-forward when a time setting switch is pressed. To make the time setting speed up, it is necessary to make the reference clock frequency higher than 60Hz. By making the clock signal bypass the 1-second divider, time setting is speeded up by 60 times. Even so, it would still take 20 minutes to advance the time for 24 hours. To make it advance still faster, the 10-minute frequency divider is also bypassed. Thus the 1-second frequency divider bypassing switch is used for "slow" adjustment and the 10-minute frequency divider bypassing switch for "fast" mode.

This way, it only takes a little more than two minutes to make a full 24-hour adjustment. However, these fast-forward switches cannot make second adjustment. 0-second setting can be made by pressing the "0-second Set" switch and clearing the second counter until the correct second appears. Fig. 75 shows the block diagram of a digital clock.

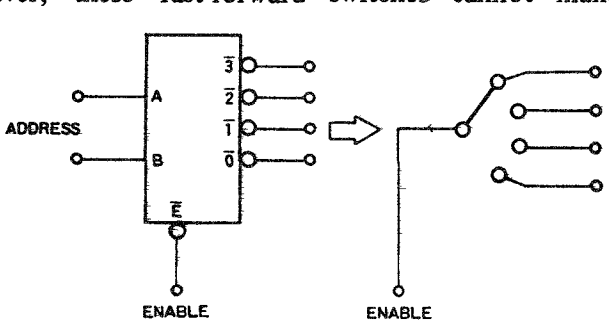


Fig. 74 Decoder with enable terminal (de-multiplexer)

The counter can be asynchronous. An SN7490 can be used for a quinary-decimal counter and an SN7492 for a hexal type. Making a 24-radix counter only is meaningless, since BCD output is necessary for indicating time. The output can be made with the remaining binary counter portions of the SN7490 and SN7492 along with one or two gates.

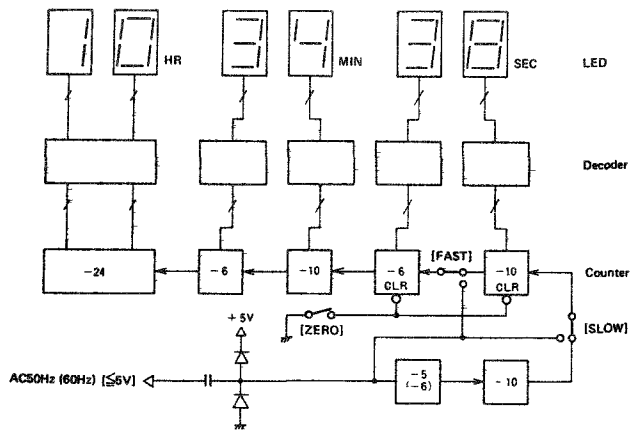
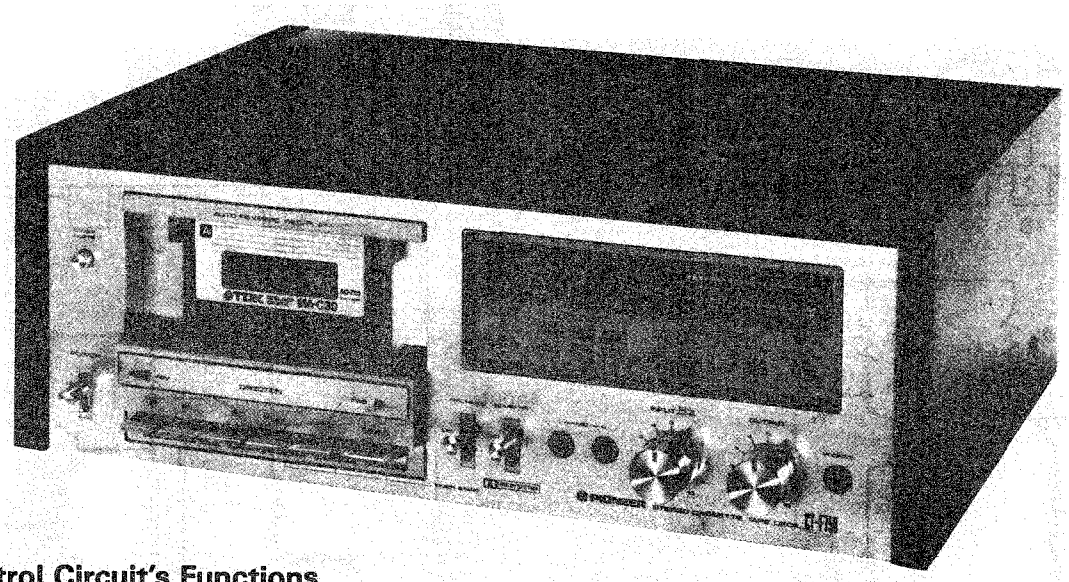


Fig. 75 Block diagram of digital clock

Application Course (1)

CT-F750

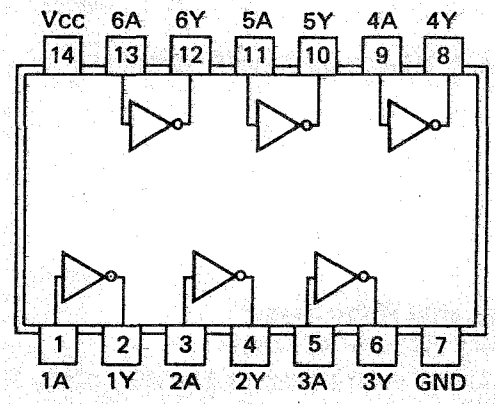


1. Control Circuit's Functions

1-1. IC's employed

Inverter

M53204P (TI's SN7404N)



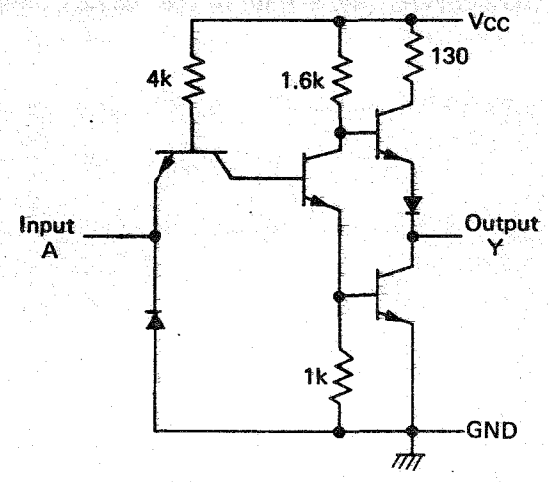
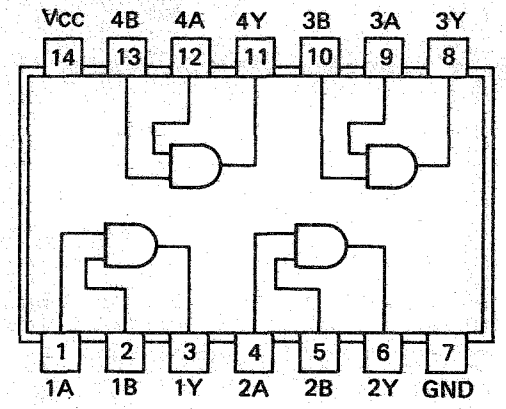


Fig. 1 Inverter M53204P (SN7404N)

AND

M53208P (TI's SN7408N)



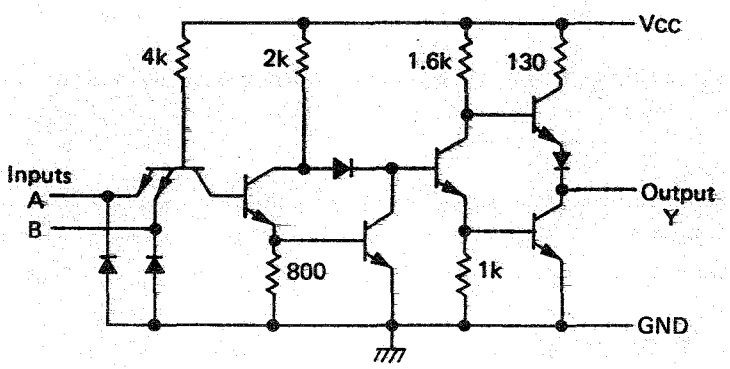


Fig. 2 AND Circuit M53208P (SN7408N)

NAND
M53200P (TI's SN7400N)

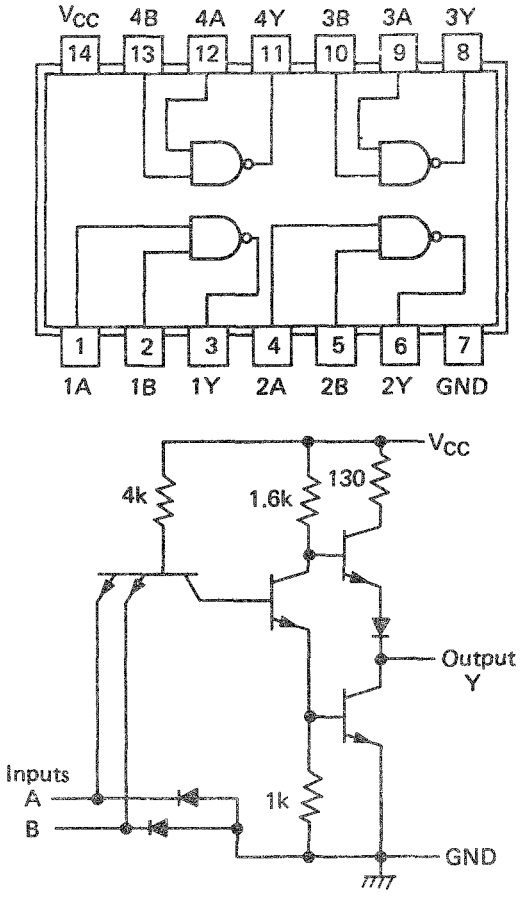


Fig. 3 NAND Circuit M53200P (SN7400N)

NOR
M53202P (TI's SN7402N)

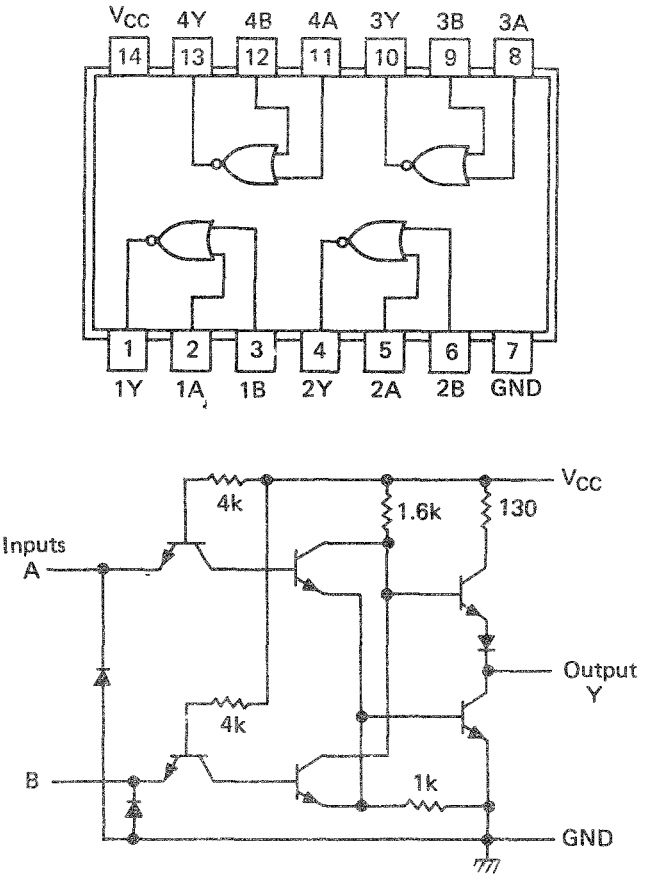


Fig. 4 NOR Circuit M53202P (SN7402N)

1-2. One-shot Multivibrator
M53321P (TI's SN74121N)
For detailed descriptions of Inverter, AND, NAND and NOR circuits, please refer to the "Basic Course."

1-3. One-Shot Multivibrator M53321P's functions

This One-Shot Multivibrator puts out a pulse signal when certain input conditions are satisfied. The pulse width of the M53321P can be adjusted by varying the value of the external capacitor and resistor.

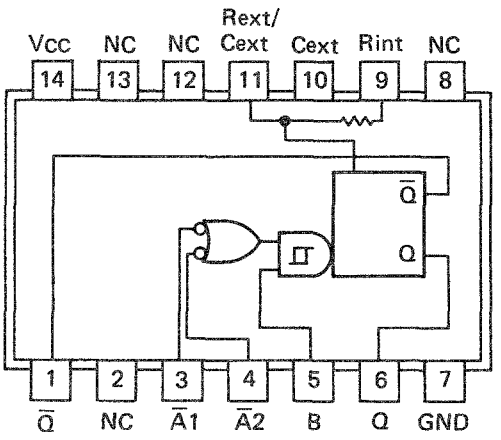
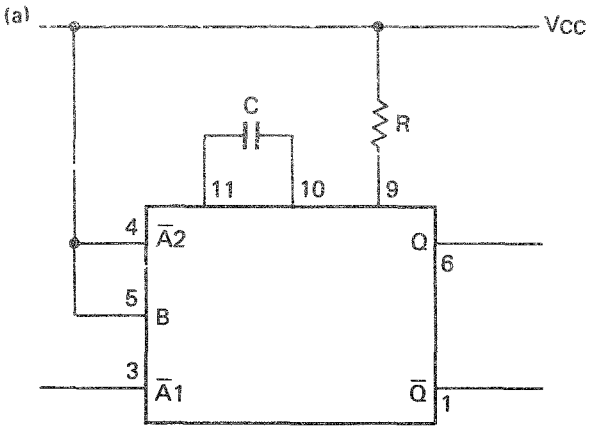


Fig. 5 Pin alignment and block diagram

Inputs			Outputs	
$\bar{A}1$	$\bar{A}2$	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	↓	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

Fig. 6 Function table

There are two ways of connecting the M53321P as shown in Fig. 7:



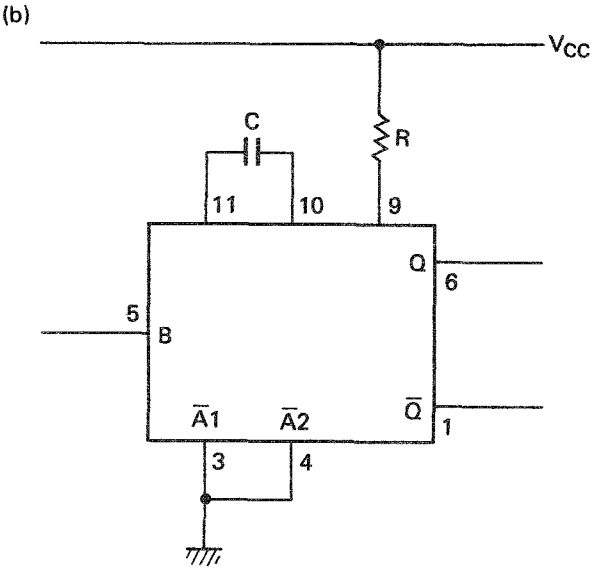


Fig. 7 Connections of M53321P

Fig. 7(a) : Terminals 4 ($\bar{A}2$) and 5 (B) are connected to Vcc which is H level. Now, refer to the function table in Fig. 6. ($\bar{A}2$) and B are always H and only when the level at 3 ($\bar{A}1$) falls to L, output 6 (Q) inverts from L to H and then returns to L after a certain period of time. A positive pulse can be obtained at Q; the pulse width is determined by the product value of the capacitor and resistor connected to the IC. The actual time constant value is different from the product value because the IC has an internal resistor. The pulse width will be explained later. The level of $\bar{Q}$ is always opposite to that of Q (refer to the "Basic Course" Section on flip-flops).

Fig. 7 (b): Terminals 3 ($\bar{A}1$) and 4 ($\bar{A}2$) remain L because they are grounded. Refer to the Function Table in Fig. 6. "X" means that the level can be either H or L. Since $\bar{A}1$ and $\bar{A}2$ are always L, a positive pulse and a negative pulse appear at 6 (Q) and 1 ($\bar{Q}$) respectively only when the level at 5 (B) rises to H. In almost all cases, the outputs of 6 (Q) and 1 ($\bar{Q}$) remain unchanged in respect to L and H, except in the following instances:

When input at 3 ($\bar{A}1$) shifts from H to L in the circuit in Fig. 7 (a).

When input at 5 (B) shifts from L to H in the circuit in Fig. 7 (b).

In each case, a pulse of a certain width appears at the output terminals, a positive pulse at 6 and a negative pulse at 1.

2. Circuit Description

2-1. Auto-Stop Circuit (solenoid activation)

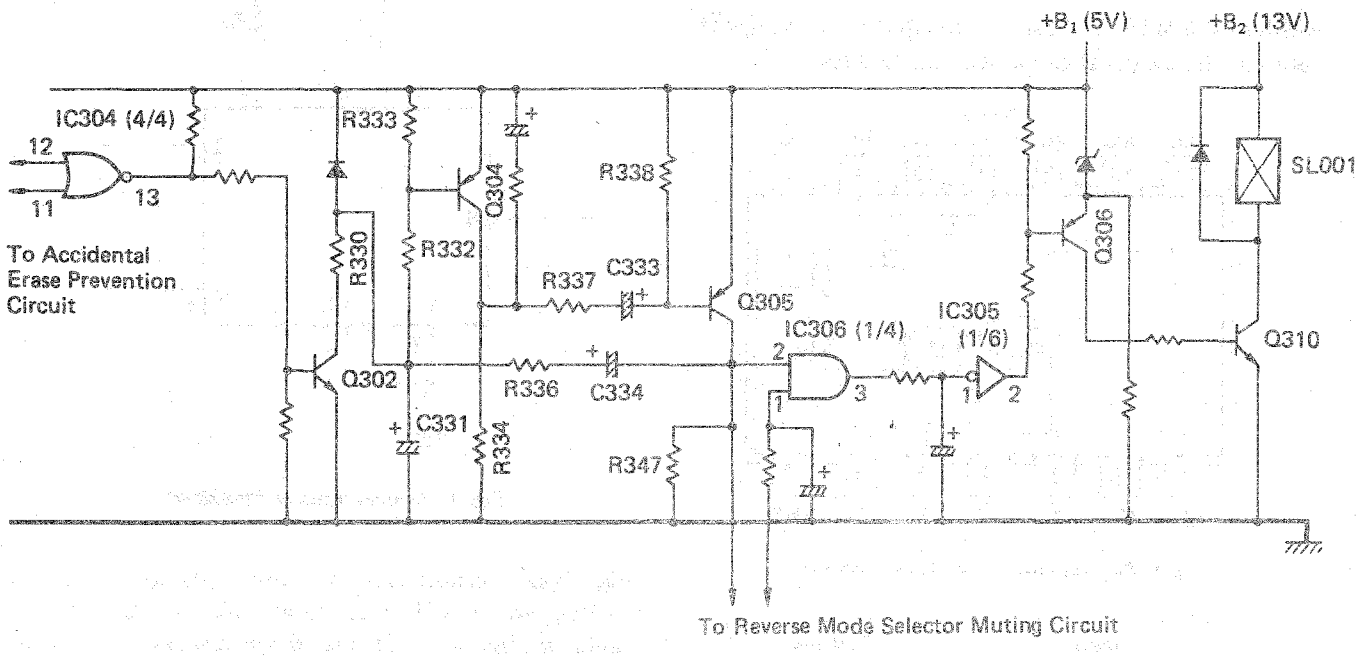
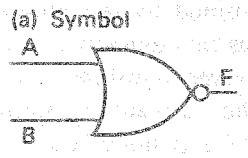


Fig. 8 Auto-Stop Circuit



(b) Function table

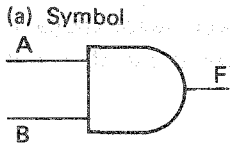
A	B	F = A + B
L	L	H
L	H	L
H	L	L
H	H	L

Fig. 9

When in the PLAY mode and PAUSE is pressed, inputs 11 and 12 of IC304 (4/4)'s NOR gate are L and output 13 becomes H (refer to Fig. 9). IC304 (4/4)'s output at 13 : H → Q302's base : H → Q302 : ON → Current flows from +B1 through R333, R332, R330 and Q302 → Q304's base : L → Q304 : ON → Collector : H → C333's terminals almost equal to +B1 → No current through R338 → Q305's base : H → Q305 : OFF → IC306 (1/4)'s input 2 : L → Output 3 : L (refer to Fig. 10) → IC305 (1/6) inverts L to H → Q306's base : H → Q306 : OFF → Q310's base : L → Auto-Stop solenoid SL001 is not activated (PLAY or PAUSE).

At the end of PLAY, FF, REW or when the Accidental Erase Prevention Circuit is activated (explained later), input 11 or 12 of NOR IC304 (4/4) becomes H and output 13 becomes L.

IC304 (4/4)'s output 13 : L → Q302's base : L → Q302 : OFF → C331 is charged through R333 and R332 → Charging completed → Current stops → Q304's base: H → Q304 : OFF → C333 is charged through R338, R337 and R334 → Q305's base : L → Q305 : ON → IC306 (1/4)'s input 2 : H. When tape stops, except when auto-reversing, (explained later) input 1 of IC306 (1/4) is H → Both inputs 1 & 2 : H → Output 3 : H → Inverter IC305 (1/6)'s output : L → Q306's base : L → Q306 : ON → Q310's base : H → Q310 : ON → Auto-Stop solenoid activated, tape transport stops.



(b) Function table

A	B	F = A · B
L	L	L
L	H	L
H	L	L
H	H	H

Fig. 10

Role of astable multivibrator

In the normal state, the Auto-Stop solenoid becomes activated when an L signal from IC304 (4/4) is inverted and fed to input 2 of IC306 (1/4).

However, if for some reason the main voltage drops, the solenoid may not receive enough current to drive it with enough force to trigger the tape transport stop mechanism. To assure proper operation of the stop mechanism, a multivibrator is incorporated in the Auto-Stop circuit to repeat cycling of the solenoid until the tape transport stop mechanism is completely triggered. The resistor and capacitor inserted between IC306 (1/4) and IC305 (1/6) compose a delay circuit. In this way, the muting circuit for eliminating the "click" can operate before the solenoid works.

Solenoid operation is delayed for 10 msec. The circuit operation is the same as described previously except when Q305 is ON:

When C333 is completely charged → Q305's base : H → Q305 : OFF → Collector : L → C334's charge current flows through R333, R332, R336 and R347 → Q304's base : L → Q304 : ON → Current through R338, C333, R337 and R334 stops → Q305's base : H → Q305 : OFF → C334 is recharged → Q304's base : H → Q304 : OFF.

Since this circuit is an astable multivibrator, Q304 and Q305 turn ON and OFF reciprocally. The pulse width is about 0.25 seconds with 1.75 second intervals.

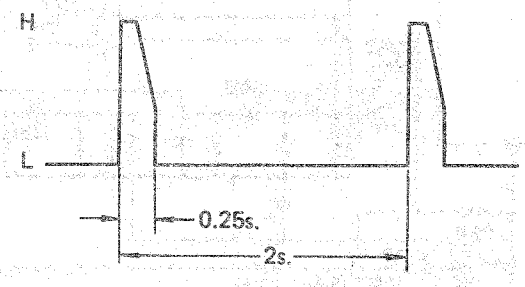


Fig. 11 Waveform of the multivibrator

2-2. Auto-Stop Detection Circuit

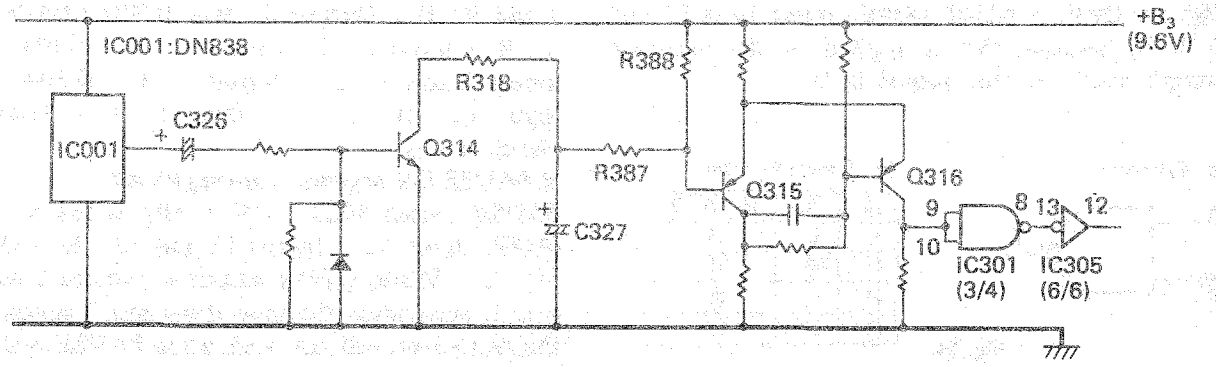


Fig. 12 Auto-Stop Sensing Circuit

When the tape is running, the magnet mounted on the countershaft rotates in proportion to the tape speed → Pulses generated by the magnet's rotation turn the Hall IC001 ON and OFF → The ON/OFF signals to Q314's base → Q314 repeats ON/OFF cycle → When Q314 is OFF, C327 is charged through R338 and R387 → When Q314 is ON, C327 discharges through R318 and Q314. As the discharging starts before charging is completed, the base of Q315 becomes L and Q315 turns ON and Q316 turns OFF. IC301 (3/4)'s inputs : L → As NAND IC301 (3/4) is wired to work as an inverter, IC305 (6/6)'s output is L.

When the tape stops, the magnet stops rotating → IC001 stops changing its ON/OFF cycles. When IC001 is OFF → Q314 remains OFF. When IC001 is ON, DC current is blocked by C326 →C327 is charged through R388 and R387 → C327 is charged completely → Q315's base : H → Q315 : OFF → Q316 : ON → IC301 (3/4)'s inputs 9 and 10 : H → IC301 (3/4)'s output 8 : L → IC305 (6/6)'s output 12 : H.

2-3. Auto-Stop Control Circuit

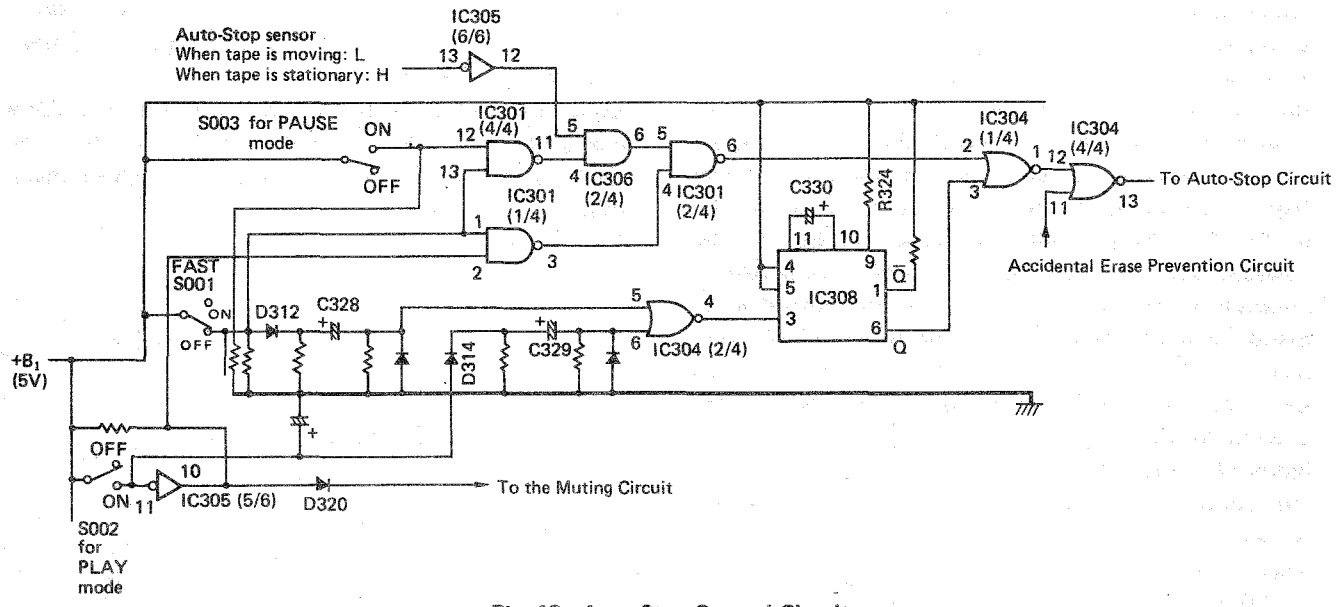


Fig. 13 Auto-Stop Control Circuit

The Auto-Stop Circuit works when either or both of the IC304 (4/4)'s inputs (11 and 12) become H (refer to 2-1). IC304 (4/4)'s input 11 is L unless the Accidental-Erase Prevention Circuit feeds a pulse to it.

a) While tape is running

When in the PLAY mode, S002 is ON and S001 and S003 are OFF. → IC301 (4/4)'s input 12 is L, and 13 is H, because +5V is applied to the terminal through S001. → The output is H.

(a) Symbol

(b) Function table

A	B	F = A · B
L	L	H
L	H	H
H	L	H
H	H	L

Fig. 14

IC301 (1/4)'s input 1 : H → IC305 (5/6) inverts the pulse from S002 → IC301 (1/4)'s input 2 : L → Output 3 : H. IC301 (4/4)'s output 11 : H → IC306 (2/4)'s input 4 : H.

While the tape is running, IC305 (6/6)'s output 12 : L → IC306 (2/4)'s input 5 : L → Output 6 : L. IC301 (1/4)'s output 3 : H → IC301 (2/4)'s input 4 : H → Input 5 : L → Output 6 : H → IC304 (1/4)'s input 2 : H. IC304 (2/4)'s output 4 : L → IC308's input 3 → IC308's output 6 (Q) is fed into IC304 (1/4)'s input 3.

When the M53321 One-shot Multivibrator is not working, output 6 (Q) is L → IC304 (1/4)'s input 3 : L and input 2 : H → Output 1 : L. Refer to Fig. 7 (a).

The Auto-Stop Circuit doesn't work because IC304 (4/4)'s inputs 11 and 12 are L and output 13 is H.

b) When tape stops

IC305 (6/6)'s output 12 becomes H (refer to 2-2 Auto-Stop Detection Circuit) → IC306 (2/4)'s inputs 4 and 5 : H → Output 6 : H → IC301 (2/4)'s input 5 : H → Input 4 : H → Output 6 : L → IC304 (1/4)'s inputs 2 and 3 : L → Output 1: H → IC304 (4/4)'s input 12 : H, 11 : L → Output : L → Auto-Stop circuit works.

c) PAUSE ON depressed during PLAY

PAUSE switch S003 : ON → $+B_1$ is fed to IC301 (4/4)'s input 12 → Inputs 12 and 13 : H → Output 11 : L → IC306 (2/4)'s output 6 remains L because 4 is L even when the tape stops and 5 becomes H, the Auto-Stop will not work when PAUSE is ON.

d) During FF/REW

FF switch S001 : ON, S002 : OFF, S003 : OFF → IC301 (4/4)'s inputs 12 and 13 : L → Output 11 : H. IC305 (5/6)'s input 11 : L → Output 10 : H → IC301 (1/4)'s input 2 : H, 1 : L → Output 3 : H. Since inputs of IC306 (2/4) and IC301 (2/4) are the same as those during PLAY → When tape stops and IC305 (6/6)'s output 12 becomes H, the Auto-Stop circuit works and the tape stops.

e) PAUSE ON during FF/REW

IC301 (4/4)'s input 13 : L → IC301 (4/4)'s output 11 is H, which is the same state as FF/REW, even when S003 is ON and input 12 is H → Auto-Stop Circuit works.

f) When playing a slack tape

When playing a slack tape or if the tape is left slack for about 3 seconds after FF/REW is shifted to PLAY skipping STOP, the Auto-Stop Sensor becomes activated. To prevent this, One-Shot Mulivibrator IC308 keeps the sensor inoperative for 5 seconds. When the tape is in the FORWARD PLAY mode, the sensor will not be activated by tape slack because the sensor is linked with the right reel, which in this case is the take-up reel. However, when reversing, the right reel becomes the supply reel, so when the tape becomes slack, the sensor stops rotatint thus activating the Auto-Stop Circuit.

PLAY : ON → S002 : ON → IC304 (2/4)'s input 6 becomes H for a short time until C329 is charged, output 4 : L (Fig. 13).

g) PLAY depressed during FF/REW

S001 : OFF → IC304 (2/4)'s input 5 becomes H for a short time by current through D312 and C328. When PLAY : ON → S002: ON → IC304 (2/4) input 6 : H for a short time. When either or both inputs 5 and 6 are H, output 4 shifts from H to L for about 70 msec. IC308 is an IC M53321P which was described earlier in Fig. 7 (a). IC308's input 3 shifts from H to L, IC308 : ON → A positive pulse with a width of 5 seconds, as determined by C330 and R324 appears at output 6 (Q), goes to IC304 (1/4) input 3. Even when the Auto-Stop Sensor is activated and IC304 (1/4)'s input 2 shifts to L, the IC's output 1 remains L as long as input 3 is H. IC304 (4/4)'s inputs 11 and 12 : L → Output 13 : H → Auto-Stop Circuit remains inoperative.

In short, for about 5 seconds when IC308's output 6 (Q) remains H, the Auto-Stop Circuit is not activated. Actually, it will take nearly 7 seconds because it takes 2 seconds more for the astable multivibrator to operate.

2-4. Trigger Control Circuit

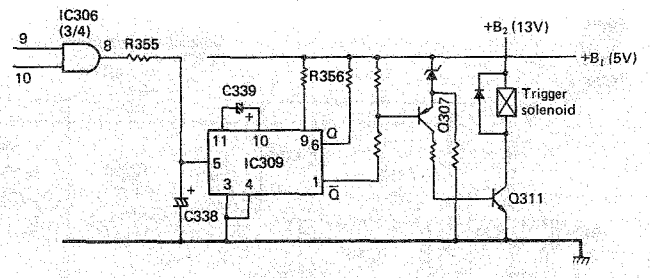


Fig. 15 Trigger Control Circuit

This circuit controls Trigger Solenoid action and switches FWD and REV. IC306 (3/4)'s input 9 is usually H unless the Accidental-Erase Prevention Circuit (explained later) works and feeds L pulse to 9. When manual or auto reversing, IC306 (3/4)'s input 10 and output 8 becomes H. When IC309's input 5 shifts from L to H, the IC309 works. [Refer to Fig. 7 (b).]

A negative pulse with a width of 0.2 sec., as determined by C339 and R356 appears at output 1 ($\bar{Q}$). → Q307's base : L → Q307 : ON → Q311 : ON → Trigger Solenoid trips. → Switches FWD/REV. (R355 and C338 compose a delay circuit which provides the necessary time lag for the Muting Circuit to eliminate the "click" sound produced by the solenoid.

2-5. Direction Selector Circuit

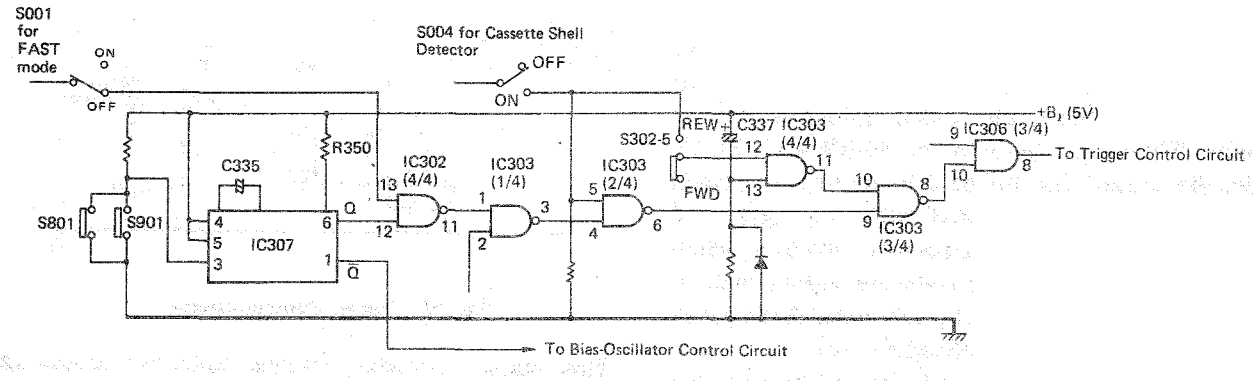


Fig. 16 Part of Direction Selector Circuit

When direction switch S801 or S901 is pressed: IC307's input 3 shifts to L → Positive and negative pulses appear at 6 (Q) and 1 ($\overline{Q}$) respectively [refer to Fig. 7 (a)]. The pulse width is 1 sec. as determined by C335 and R350. IC307's output 6 (Q) : H → IC302 (4/4)'s input 12 : H. At the time of PLAY or STOP, S001's output : H → IC302 (4/4)'s input 13 : H → Output 11 : L → IC303 (1/4)'s input 1 : L. Mode Selector signal (explained later) goes to IC303 (1/4)'s input 2 → Output 3 : H unless auto-reversing → IC303 (2/4)'s input 4 : H. When a cassette is loaded, S004's output : H → IC303 (2/4)'s input 5 : H → Output 6 : L → IC303 (3/4)'s input 9 : L → IC303 (4/4)'s output 11 : H unless the FWD Priority Circuit is activated (explained later) → IC303 (3/4)'s input 10 : H → Output 8 : H → IC306 (3/4)'s input 10 : H → Trigger Control Circuit activated.→ Switches FWD/REV.

The circuit is also designed to prevent its operation during FF/REW or when a tape is not loaded. During FF, S001 : ON → IC302 (4/4)'s input 13 : L. This time, even when S801 or S901 is depressed and IC302 (4/4)'s input 12 becomes H, output 11 remains H → Downstream IC's outputs remain unchanged → FWD/REV remains unchanged.

When a tape is not loaded, S004 : OFF → IC303 (2/4)'s input 5 : L → Output remains H even when S801 or S901 is depressed and input 4 becomes H → Downstream IC's outputs remain unchanged → FWD/REV switch does not trip.

2-6. FWD Priority Circuit (Timer-Start)

When the Timer-Start function is in use and a tape is loaded, this circuit shifts REV recording to FWD recording when the FWD/REV selector is in the REV position. (Refer to Fig. 17 Reverse Mode Selector Circuit.)

POWER : ON → S004's output : H → S302-5 : H → IC303 (4/4)'s input 12 : H. Charging current to C337 makes input 13 H and output 11 : L for a short time → IC303 (3/4)'s input 10 : L → Output 8 : H → Trigger Control Circuit works → REV shifts to FWD.

2-7. Reverse Mode Selector Circuit

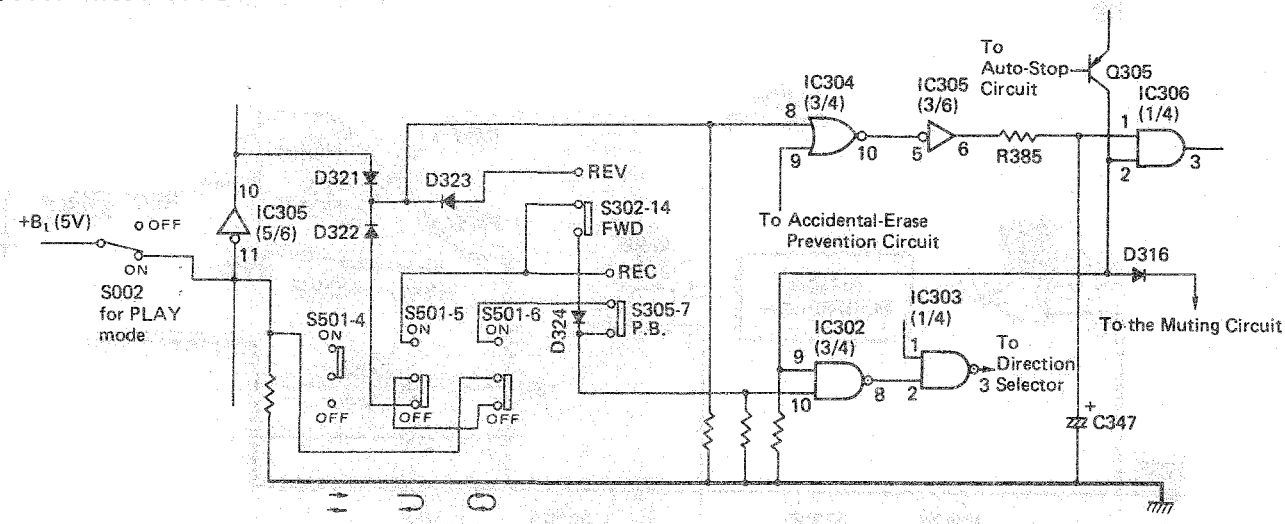


Fig. 17 Reverse Mode Selector Circuit

IC 304 (3/4)'s input 9 is usually L because it is connected to the Accidental-Erase Prevention Circuit.

a) ⇄ Mode (S501-4 : ON, S501-5 : OFF, S501-6 : OFF)

S002 ON : H → S501-6 : OFF : H → S501-5 : OFF : H → D322's output : H → IC304 (3/4)'s input 8 : H → Output 10 : L → IC305 (3/6) inverts to H → IC306 (1/4)'s input 1 : H. When tape ends, Q305 : ON (refer to 2-1) → IC306 (1/4)'s input 2 : H → 3 : H → Auto-Stop circuit activates → STOP solenoid operates. At this time, IC302 (3/4)'s input 10 : L → Q305 : ON → IC302 (3/4)'s input 9 : H → output 8 : H → IC303 (1/4)'s 2 : H → Input 1 : H unless Direction Button is pressed → Output 3 : L → Direction Selector Circuit deactivated.

b) ⊃ Mode (S501-4 : OFF, S501-5 : ON, S501-6 : OFF)

(1) ⊃ Directon

In the FWD mode : H signal goes to IC302 (3/4)'s input 10 through S002, S501-6, S501-5 and S302-14 and D324. When tape ends → Q305 : ON → Input 9 : H → Output 8 : L. IC303 (1/4)'s inputs 1 & 2 are usually H and L respectively → Output 3 : H → Direction Selector shifts to REV. Here, IC304 (3/4)'s input 8 : L → input 9 : L → output 10 : H → IC305 (3/6) inverts to L → IC306 (1/4)'s input 1 : L → Output 3 : L → Auto-Stop mechanism deactivated.

(2) ⊂ Direction

When reversing : H signal goes to IC304 (3/4)'s input 8 via S002, S501-6, S501-5, S302-14 and D323. → Output 10 : L → IC305 (3/6) inverts → IC306 (1/4)'s input 1 : H. Q305 : ON at tape end → Input 2 : H → Output 3 : H → Auto-Stop Circuit operates. (The same as in the ⇄ mode). At this time, the direction shifter does not operate because IC302 (3/4)'s input 10 is L.

c) ⊂⊃ Mode (S501-4 : OFF, S501-5 : OFF, S501-6 : ON)

During PLAY : H signal goes to IC302 (3/4)'s input 10 through S002, S501-6 and S305-7. At tape end, Q305 : ON → IC302 (3/4)'s 9 : H → Output 8 : L → Tape Direction selector works. At this time, Auto-Stop does not operate because IC304 (3/4)'s input 8 remains L regardless of the FWD/REV direction. The tape runs endlessly.

In RECORD : Similar circuit as in ⊃ mode to prevent accidental recording: When REV RECORD is depressed, Auto-Stop operates. When forwarding, via D324 : H → IC302 (3/4)'s input 10 : H → Direction Selector operates. When reversing via D323 : H → IC304 (3/4)'s input 8 : H → Auto-Stop operates.

d) Role of D321

D321 is employed to give Auto-Stop preference over FF/REW. S002 is OFF at FF/REW. This time, IC305 (5/6)'s input 11 : L → Output 10 : H → via D321 : H → IC304 (3/4)'s input 8 : H → Auto-Stop operates. Here, S002 : OFF → IC302 (3/4)'s input 10 : L at any position → Direction Selector unchanged.

e) Role of R385 and C347

When auto-reversing from FWD to REV at tape end, S302-14 switches from FWD to REV (refer to ⊂⊃ mode) → D323 : H → IC304 (3/4)'s input 8 : H → IC306 (1/4)'s input 1 : H. The mechanical switching time, about 0.3 sec., serves as the delay time. Q305 stays ON for 0.25 sec. (refer to Auto-Stop Circuit). S302-14's sliding time and multivibrator's delay time have allowances. If the switch slides earlier than the time Q305 goes off, IC306 (1/4)'s inputs 1 and 2 become H and the Stop solenoid operates unexpectedly. To prevent this, R385 and C347 delay the shifting time of IC306 (1/4)'s input 2 to H for about 0.5 sec.

2-8. Accidental-Erase Prevention Circuit

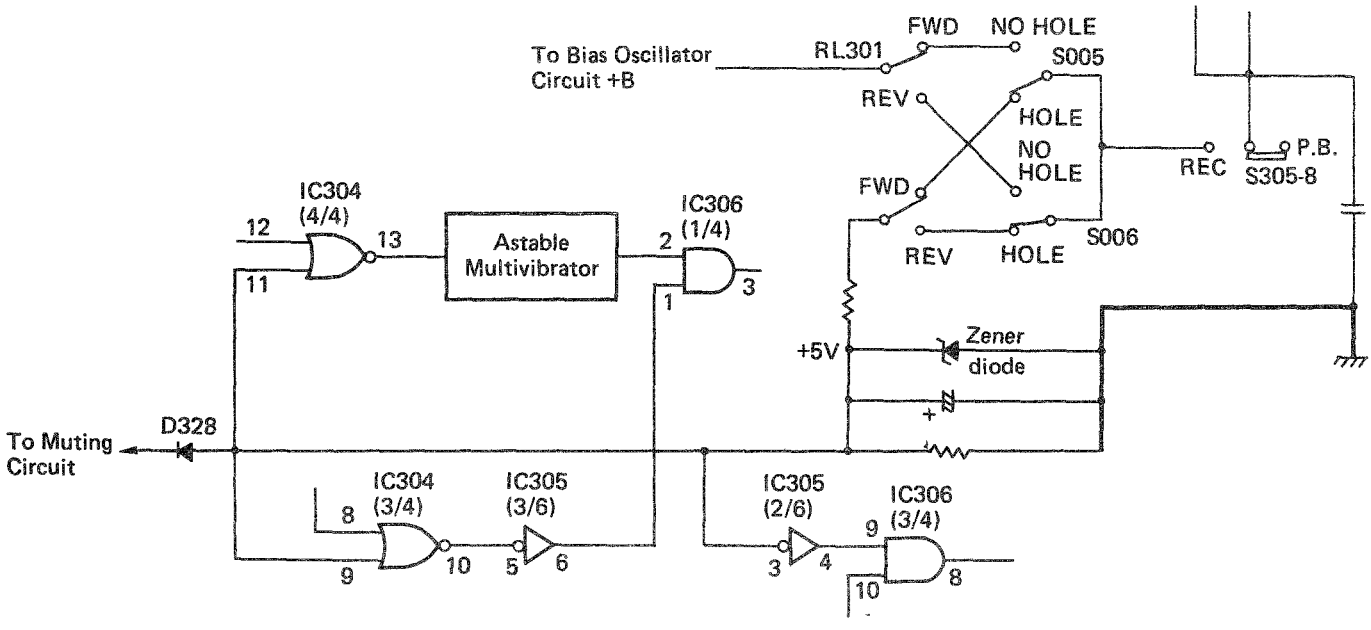


Fig. 18 Accidental-Erase Prevention Circuit

CT-F750's Accidental-Erase Prevention is electronically controlled and its REC button can be depressed even when a cassette has no erase tab.
When the REC button is depressed after inserting a cassette which has no erase tab: S305-8 (REC) : H → S005, (S006) : H → via RL301 → IC305 (2/6)'s input 3 : H → IC304 (4/4)'s input 11 : H → Output 13 : L → Astable multivibrator operates. IC304 (3/4)'s input 9 : H → Output 10 : L → IC305 (3/6) inverts → IC306 (1/4)'s input 1 : H → Auto-Stop operates and prevents erasing. IC305 (2/6) inverts signal → IC306 (3/4)'s input 9 : L → Output 8 : L → Prevents Trigger control from operating.

2-9. Bias Oscillator Controller and Muting Signal Detector

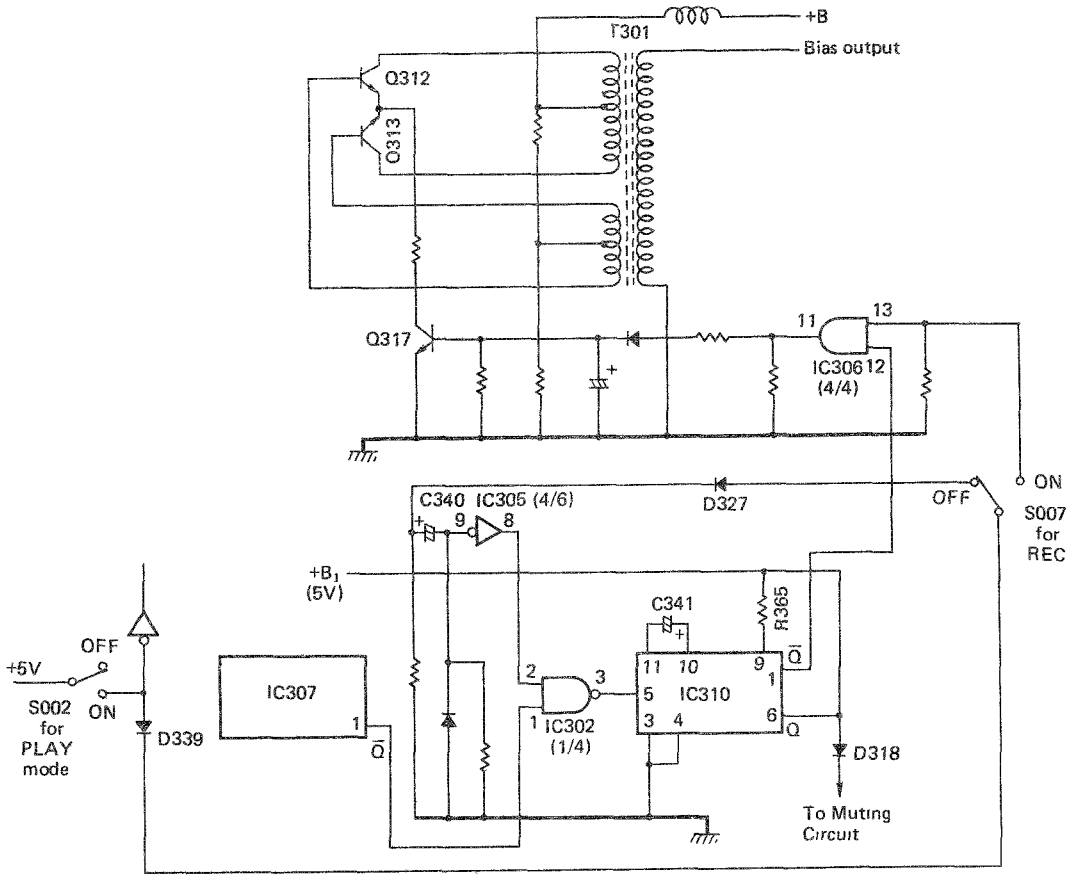


Fig. 19 Bias Oscillator Controller and Muting Signal Sensor

When REC & PLAY are depressed simultaneously, the deck starts recording: S007 and S002 : ON → IC306 (4/4)'s input 13 : H → 12 : H when IC310 is not working → IC306 (4/4)'s output 11 : H → Q317's base : H → Q317 : ON → Bias Oscillator operates → Recording starts.

When STOP & PLAY are depressed simultaneously while recording, it shifts from REC to PLAY rapidly. S007 : OFF → IC306 (4/4)'s input 13 : L → Output 11 : L → Q317's base : L → Q317 : OFF → Bias Oscillator stops (Recording stops). → PLAY starts.

The lower half of the circuit in Fig. 19 is the Muting Signal Sensor for preventing "click" noise generated by S007 and REC/PB switches on the signal channel which shift from ON to OFF, and from REC to PLAY, respectively.

S007 : OFF → C340 is charged. →IC305 (4/6)'s input 9 : H → Output 8 : L → IC302 (1/4)'s input 2 : L → IC302 (1/4)'s input 1 : H when IC307 is not working, output 3 : H → IC310's input 5 : H → IC310's [refer to Fig. 7 (b)] output 6 (Q) : H → Muting Circuit operates. The pulse width is about 1 sec. as determined by C341 and R365. This circuit also stops bias oscillation for a short time when shifting direction manually.

When shifting direction manually during recording IC307 works. → Output 1 ($\overline{Q}$) : Negative pulse (1 sec.) → IC302 (1/4)'s input 1 : L for 1 sec. → Output 3 : H → IC310 operates → Output 6 (Q) : Positive pulse (1 sec.) → Muting Circuit. At the same time IC310's output 1 ($\overline{Q}$) : Negative pulse → IC306 (4/4)'s input 12 : L for 1 sec. → Output 11 : L → Bias Oscillation stops for about 1 sec.

During Playback, muting operation is the same as above, but IC306 (4/4) does not work.

Now, you will find that there are no +B (power supply) and Ground symbols in the digital circuit diagrams. They are generally omitted. Terminals 7 and 14 of all digital IC's explained here are connected with +B and Ground respectively (refer to Fig. 1 and Fig. 5).

3. Troubleshooting Digital IC's

All digital IC's employed in CT-F750 are TTL type and pulses are generated by one-shot (mono stable) and astable multivibrators, with a width of 0.2 ~ 5 sec. is wide enough to swing the multimeter pointer. Therefore, conditions of the IC's can be checked by a conventional multimeter (10kΩ/DCV) except that the delay circuit and rise-time require an oscilloscope equipped with a memory circuit. The H level of TTL IC is +5V (4.75~5.25), the supply voltage should be 5V. With this in mind, the voltage of the stabilizing IC (TA78005P or μPC14305H) and zener diode (WD-050) should be checked first because supply voltage over 5.5V will damage the IC's while a voltage lower than 4.57V will not operate the IC's.

3-1. TTL IC Damage

A defective IC may either be "open circuited" or "shorted" because they are composed of transistors and diodes as shown in Figs. 1 ~ 4.

a) Open input terminal

When an input terminal inside is open, the IC functions as if the imput is H even when it is L because the inner level is H.

b) Shorted input (resistance 0 to 30 ohms)

Input shorting makes the IC's own input L and further makes the output of the foregoing stage L. The word "or" in the flow charts shown later refers to shorting.

c) Open output (incomplete L)

Incomplete L causes malfunction. An open circuit between output and ground or shorting between Vcc and the transistor's output will keep the IC's output high.

d) Shorted ouptut (incomplete H)

Imcomplete H is also a sign of IC malfunction. Incomplete H can be caused by transistor shorting between output and ground or an open circuit between Vcc and output, diodes and resistors.

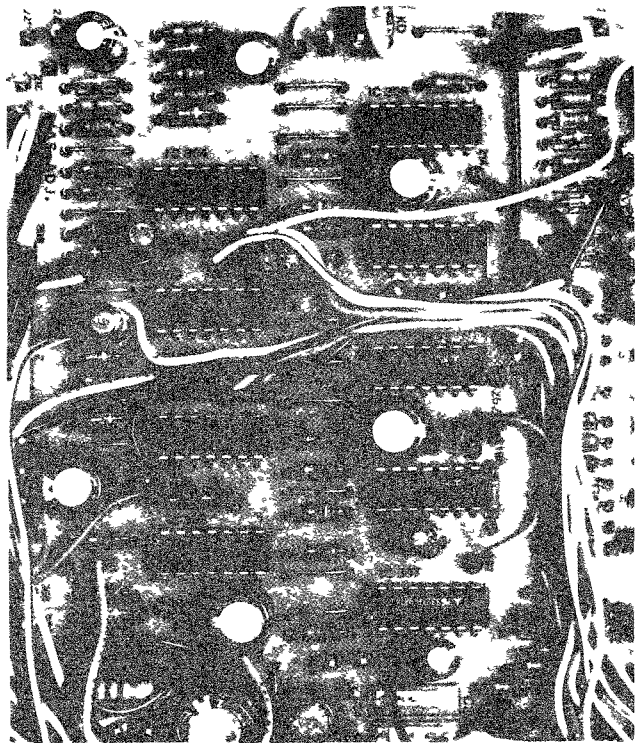
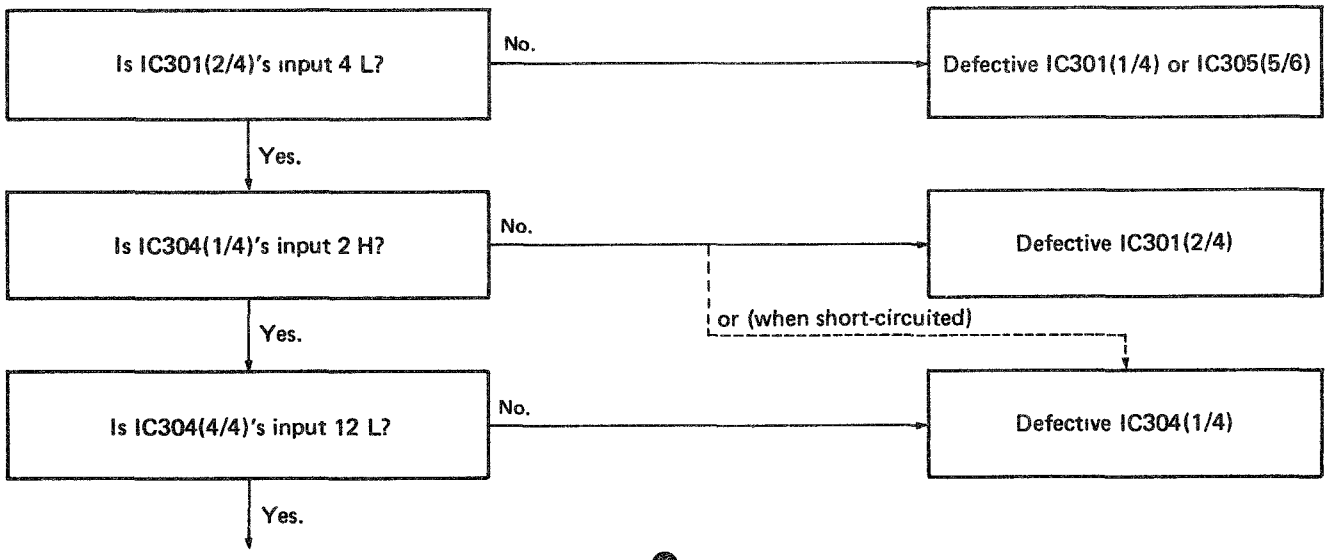
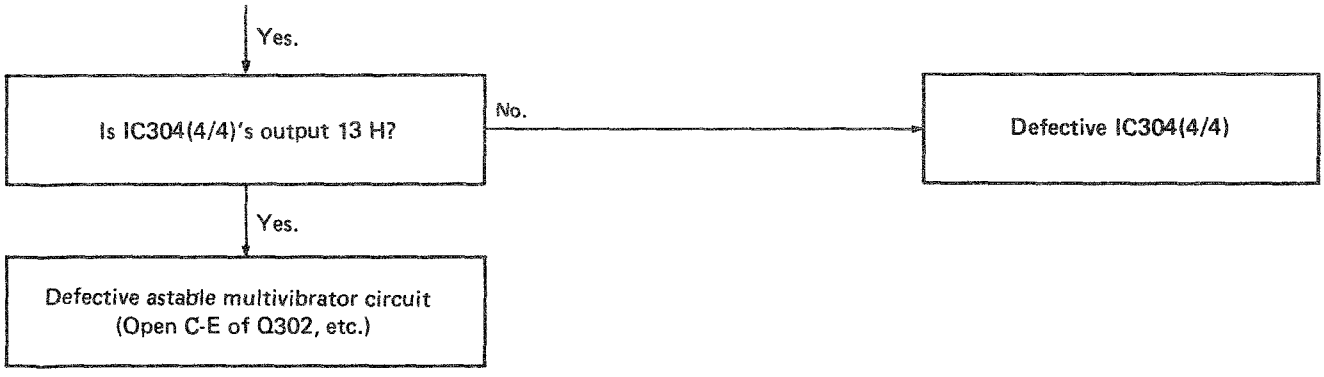


Photo of circuit board showing location of IC's

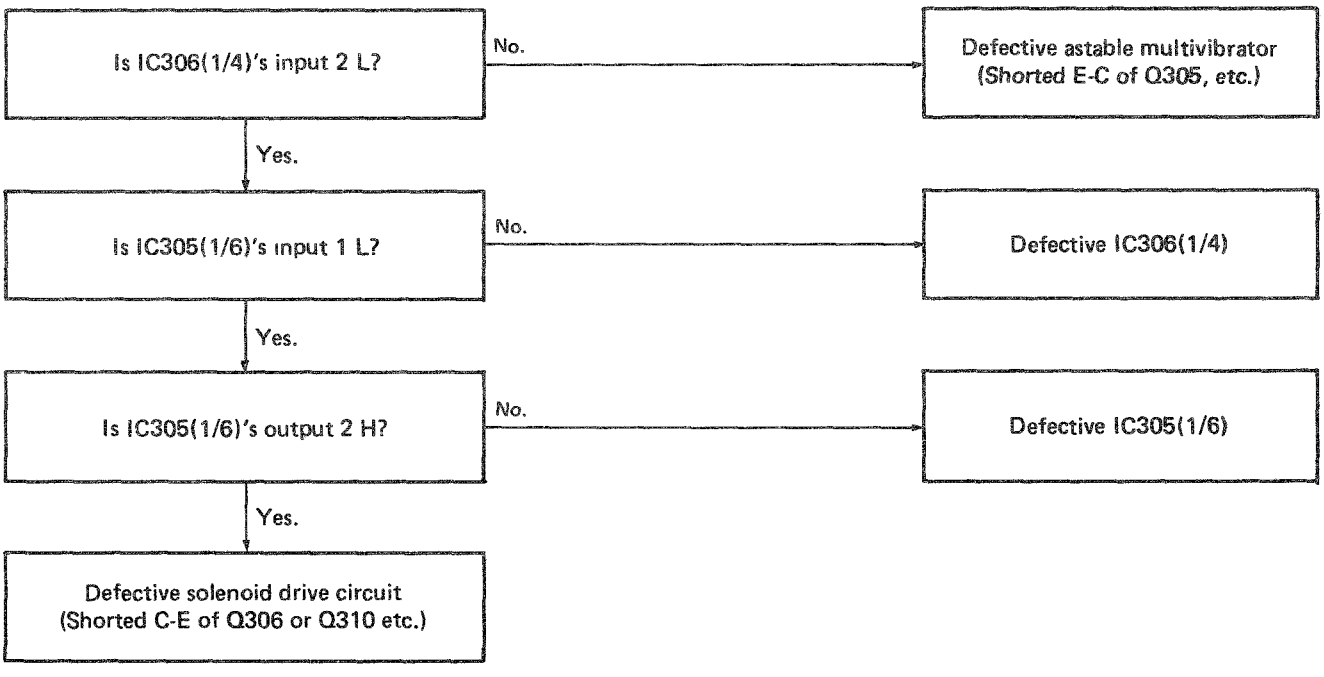
3-2. Troubleshooting Charts

a) Auto-Stop solenoid works every 2 sec. after power is turned ON.

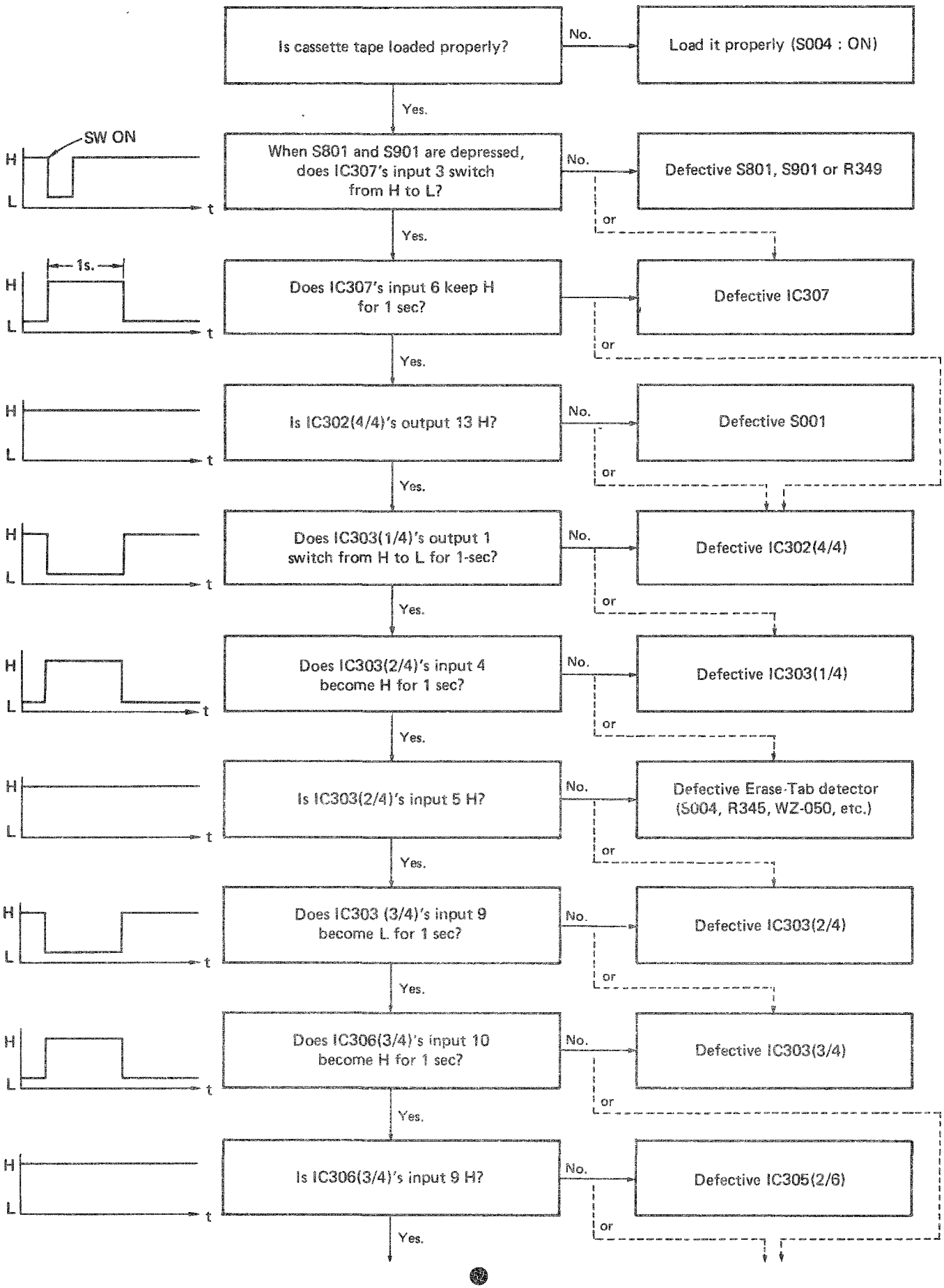


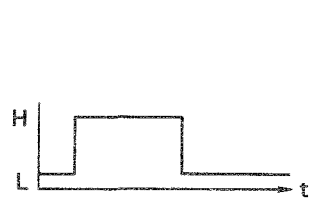


b) PLAY button doesn't lock. (Auto-Stop keeps engaging)



c) Direction selection unswitchable (manual)





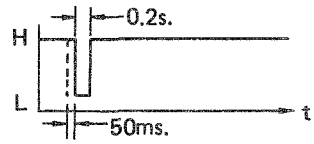
Does IC309's input 5 become H for 1 sec?

No.

Defective IC306(3/4)

or

Yes.



Does IC309's output 1 become L for 0.2 sec?

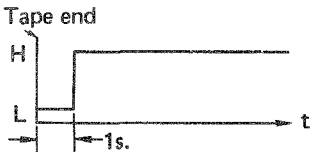
No.

Defective IC309

Yes.

Defective solenoid (SL002) or Drive circuit (Q307, Q311, etc.)

d) Auto-Stop malfunctions



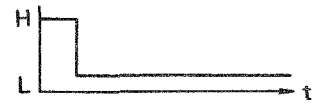
Do IC301(3/4)'s inputs 9 and 10 become H for 1 sec. after tape ends?

No.

Defective Hall IC(DN838) or Schmitt circuit (Q314, Q315, Q316, etc.)

or

Yes.

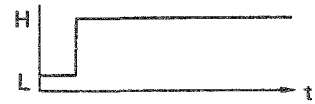


Does IC305(6/6)'s input 13 become L for 1 sec. after tape ends?

No.

Defective IC301(3/4)

Yes.



Does IC306(2/4)'s input 5 become H for 1 sec. after tape ends?

No.

Defective IC305(6/6)

or

Yes.

Is IC306(2/4)'s input 4 H?

No.

Defective IC301(4/4)

or

Yes.

Does IC301(2/4)'s input 5 become H for 1 sec. after tape ends?

No.

Defective IC306(2/4)

or

Yes.

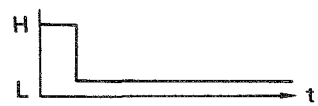
Is IC301(2/4)'s input 4 H?

No.

Defective IC301(1/4) or IC305(5/6)

or

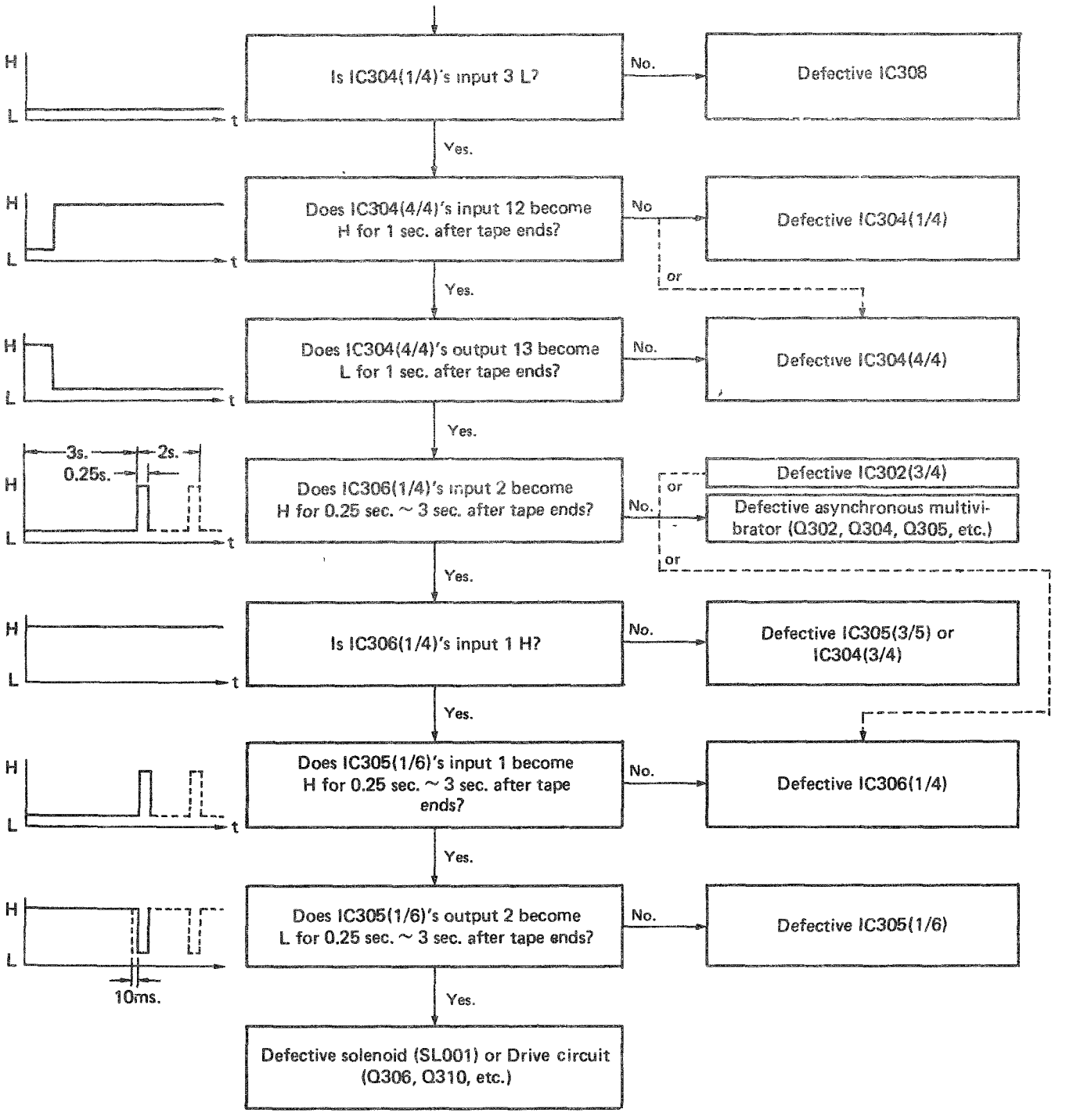
Yes.



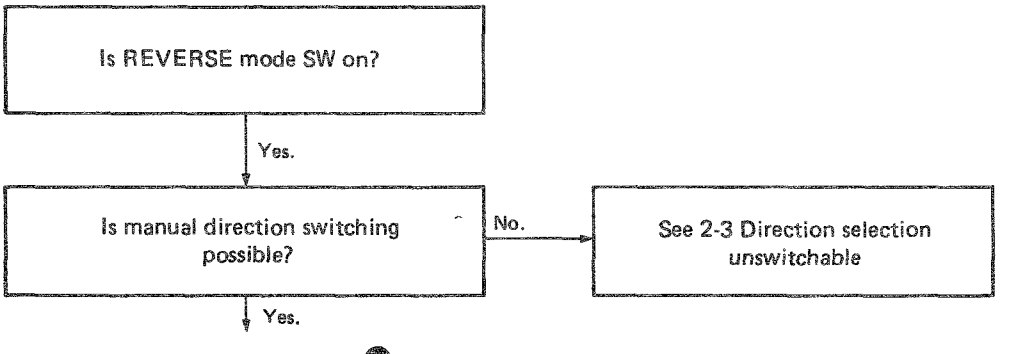
Does IC304(1/4)'s input 2 become L for 1 sec. after tape ends?

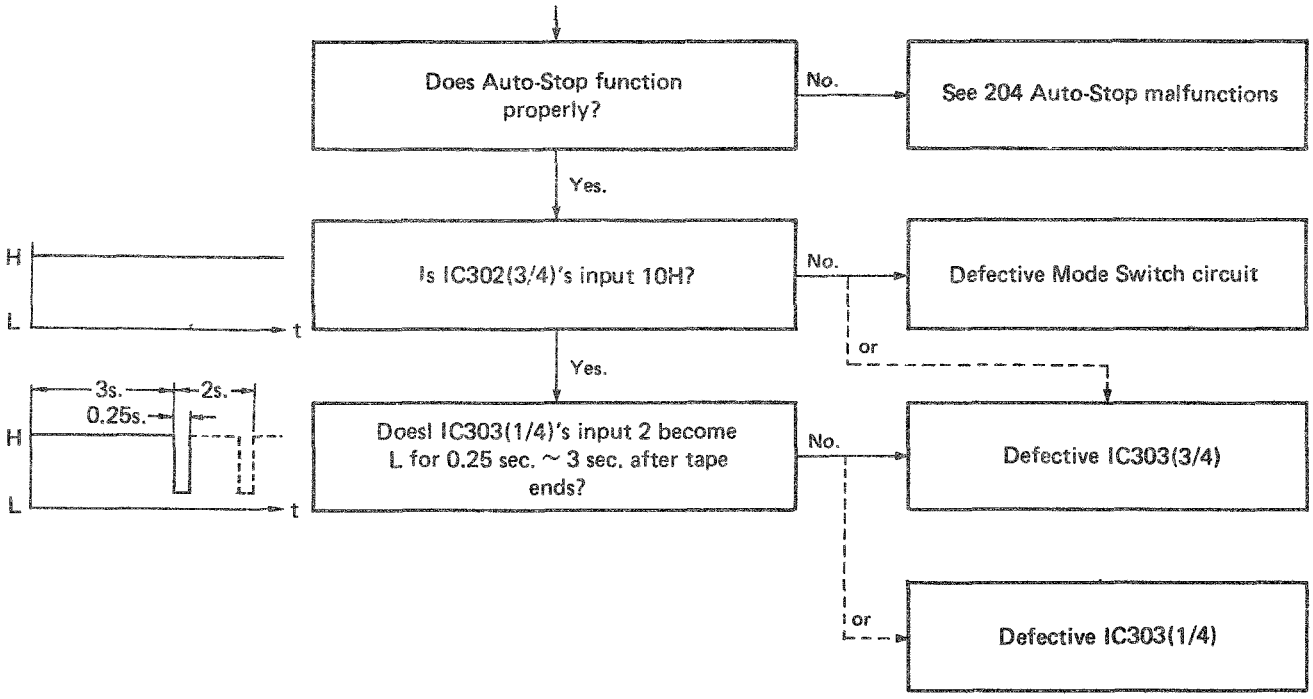
No.

Defective IC301(2/4)



e) Auto-Reverse does not function




Does Auto-Stop function properly?
No.
See 204 Auto-Stop malfunctions
Yes.
H
L
t
Is IC302(3/4)'s input 10H?
No.
Defective Mode Switch circuit
or
Yes.
3s.
2s.
0.25s.
H
L
t
Doesl IC303(1/4)'s input 2 become L for 0.25 sec. ~ 3 sec. after tape ends?
No.
Defective IC303(3/4)
or
Defective IC303(1/4)

Application Course (2)

KE-2000

1. KE-2000

To change the tuning frequency, the capacitance or the inductance are increased or decreased in value as tuning frequencies are determined by the formula:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

In the electronic tuner, a varicap (variable capacitance diode) is used in place of a capacitor. In order to change the tuning frequency, the capacitance of the varicap is adjusted by varying the DC (direct current) applied voltage.

In conventional electronic-type tuners, the potentiometer consists of VR's or semifixed VR's (variable resistor). A desired voltage is obtained by dividing the power source voltage. Later we will explain this principle in more detail as it applies to the tuner section of the KE-2000 (KE-2300).

In the case of the KE-2000, instead of dividing the power source voltage, pulses are generated both in the memory stages to get DC voltage. This method is called the voltage synthesizer system and will be explained later centering on CPU (central processor unit) IC (PD1002).

Conventional preset-memory systems use a continuously variable analog system, whereas the KE-2000 (and KE-2300 with longwave) employs a digital system which remembers frequencies by counting tuning pulses one by one; the entire process is performed electronically.

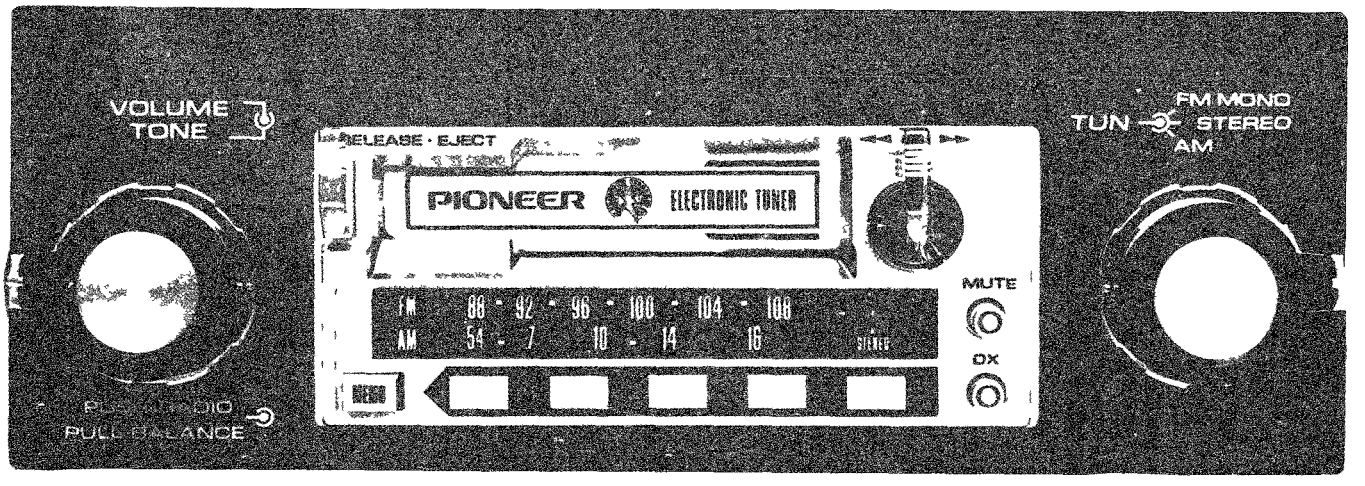


Photo 1 KE-2000

1-1. Tuning Pulse Generation

On FM dial scales, stations appear every 200kHz*. In other words, there are stations with frequencies of 98.2MHz, 99.4MHz and so on. On the other hand, you won't find stations with frequencies of 88.35MHz or 97.25MHz. So, theoretically, the following number of FM stations can be contained within a 20[MHz] (88[MHz] ~ 108[MHz]) range:

20,000[kHz] ÷ 200[kHz] = 100 stations

In general, there will be no problem with reception if there are 100 tuning points. However, to obtain accurate tuning, the use of a precise frequency division must be maintained. If the number of generated pulses (tuning points) is small, there is a greater chance of tuning error due to miscounting. If the number of generated pulses is large, frequency error can be reduced, however, both the counter and memory unit must offer high performance.

The pulse generating device, the source of digital pulses, is shown in Fig. 1 and Photo 2.

The gears mounted on the pulse generating device have a 10 to 1 ratio in respect to the tuning knob. Therefore, by turning the tuning knob a little more than eight revolutions, more than 2,000 gear teeth cross the path of the LED and phototransistor coupler, generating pulses electrooptically.

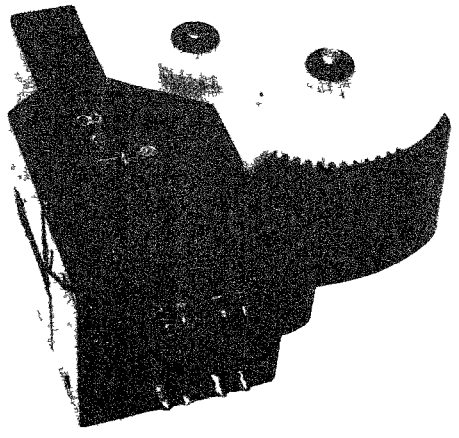


Photo 2

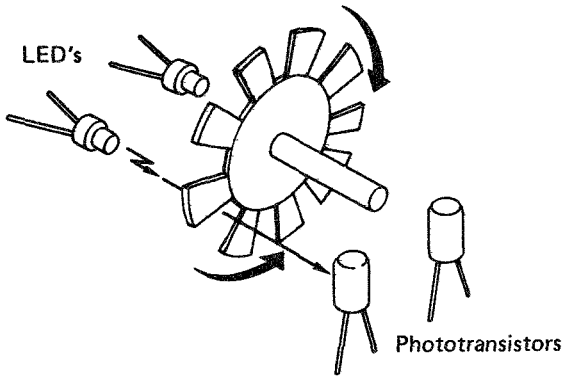
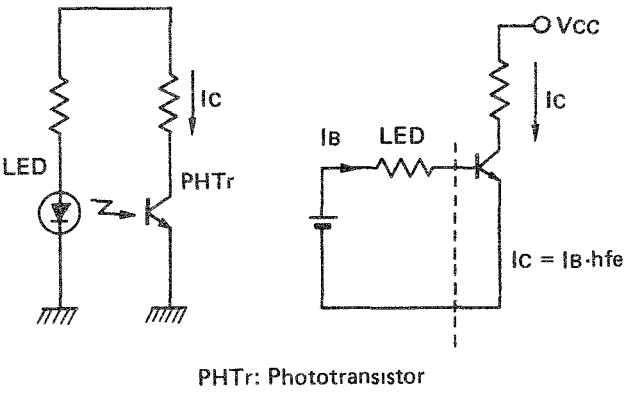


Fig. 1 Pulse generating device



PHTr: Phototransistor

Fig. 2 The phototransistor switches ON when it receives light emitted by the LED

LED's were selected as the light emitting source because of their low heat generation and long life. Though the light emitted by the LED is not visible, the wavelength is perceptible by the phototransistor.

* In some European countries, stations appear every 50kHz or 100kHz.

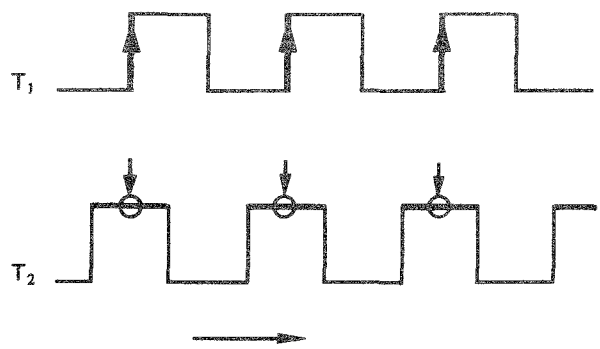
1-2. Up/Down Counter

With this device, the pulses generated by the photo couplers are counted. However, this device is unable to detect whether the tuning knob is being turned right (in the direction of higher frequencies) or left (lower frequencies) in its present state. Therefore, a pair of photocouplers (T_1 and T_2) are used, each mounted electrically 90° out of phase. This enables the device to determine whether the U/D counter's output is high or low with the edge of the clock pulse.

For detecting the "lead" or "lag" of these two pulses, a phase comparator is used. Pulses generated at T_1 and T_2 are fed separately into the C/K input and the U/D input, respectively, as clock and up/down pulses.

input and the U/D input, respectively, as clock and up/down pulses.

a) Clockwise rotation of tuning knob (Up counter)



b) Counterclockwise rotation of tuning knob (Down counter)

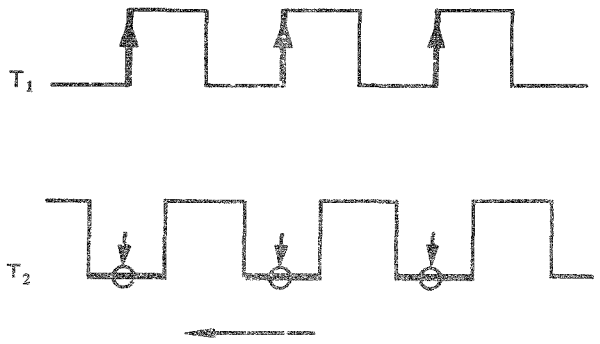


Fig. 3

Fig 3 (a) shows what occurs when the tuning knob is rotated clockwise to tune to higher frequencies. At the rise of the T_1 wave, T_2 pulses are at the H level. When T_1 (C/K) pulses are added one after another while T_2 pulses are H, we have an Up counter. When the tuning knob is rotated counterclockwise, T_2 will be at the L level at the rise of T_1 as shown in Fig. 3 (b). With this, the U/D counter commands can now be used to subtract the accumulated pulses by the number of pulses generated.

The width of each generated pulse is regulated to coincide with the rotational speed of the tuning knob and gear spacing. When knob rotation pauses, the counter stops and stores the number of pulses counted. Moreover, the feel of the tuning knob rotation is similar to that of conventional dial-pointer systems, but without tuning backlash.

The U/D counter will be explained in more detail in a later chapter

1-3. Generation of Voltage

Pulses counted by the U/D counter are then transformed into direct current (DC hereafter) corresponding to the reading of the counter (2048 max.) and it is then fed to the varicap in the front-end stage. In other words, 2048 levels of voltage can be generated by the counter.

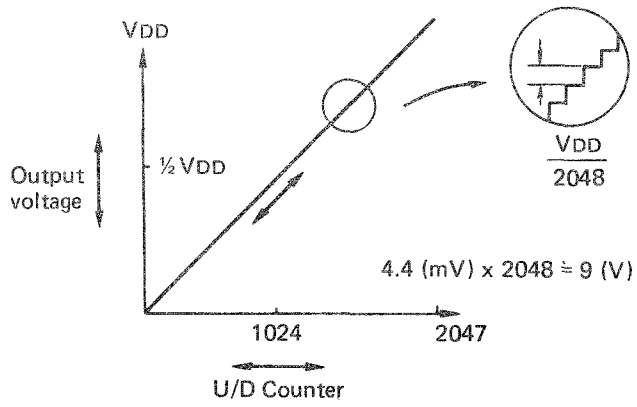


Fig. 4 Number of pulses vs. output voltage. Each step is 4.4mV

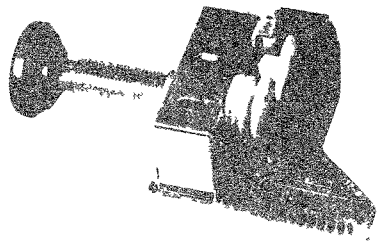


Photo 3 Pulse generator

1-4. Memory Counter

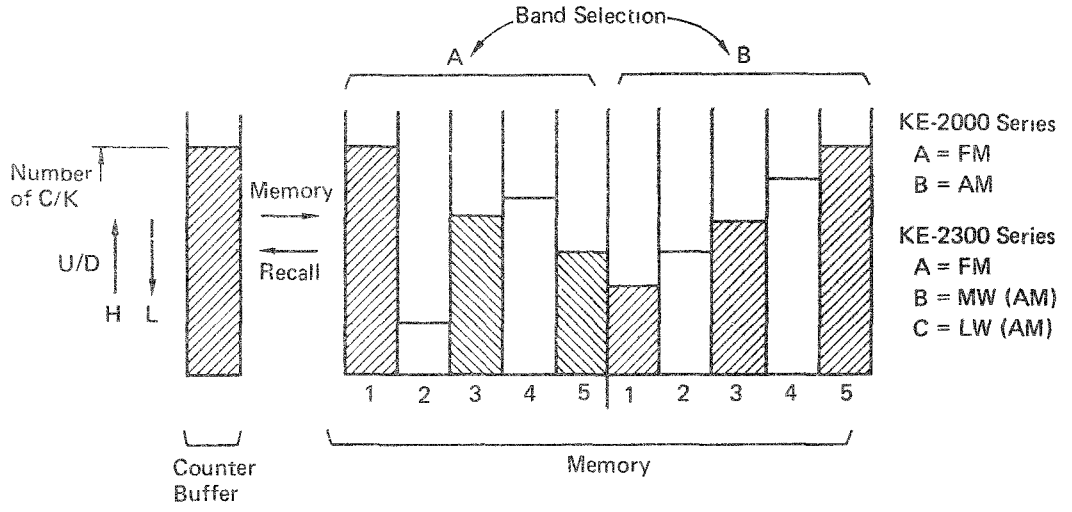


Fig. 5

The memory counter employs flip-flops. A memory buffer is used both for reading and display, however, direct reading from the memory circuit is not available.

1-5. LED's for Station Indication

In accordance with the counter reading, the 32-element LED station indicator switches on the corresponding LED's to display the selected station. (Refer to Table 6)

Table 1

LED	Counter reading	Frequency range
1	0 ~ 63	88.03 ~ 88.655
2	64 ~ 127	88.656 ~ 89.28
3	128 ~ 191	88.281 ~ 89.605
.		.
.	.	.
	.	.
	.	.
31	1920 ~ 1983	106.75 ~ 107.374
32	1984 ~ 2047	107 375 ~ 108.00

2. Control Circuit

2-1. Control Circuit

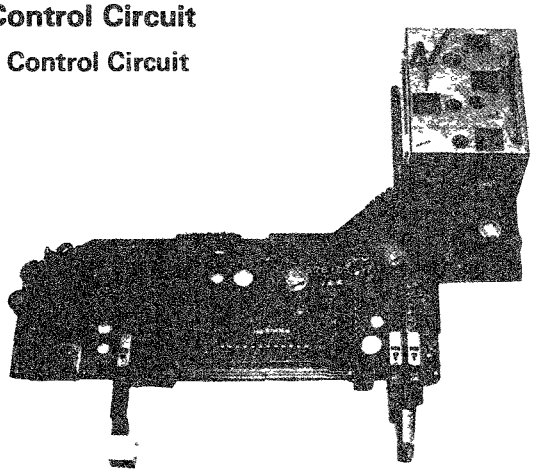


Photo 4 Control Circuit

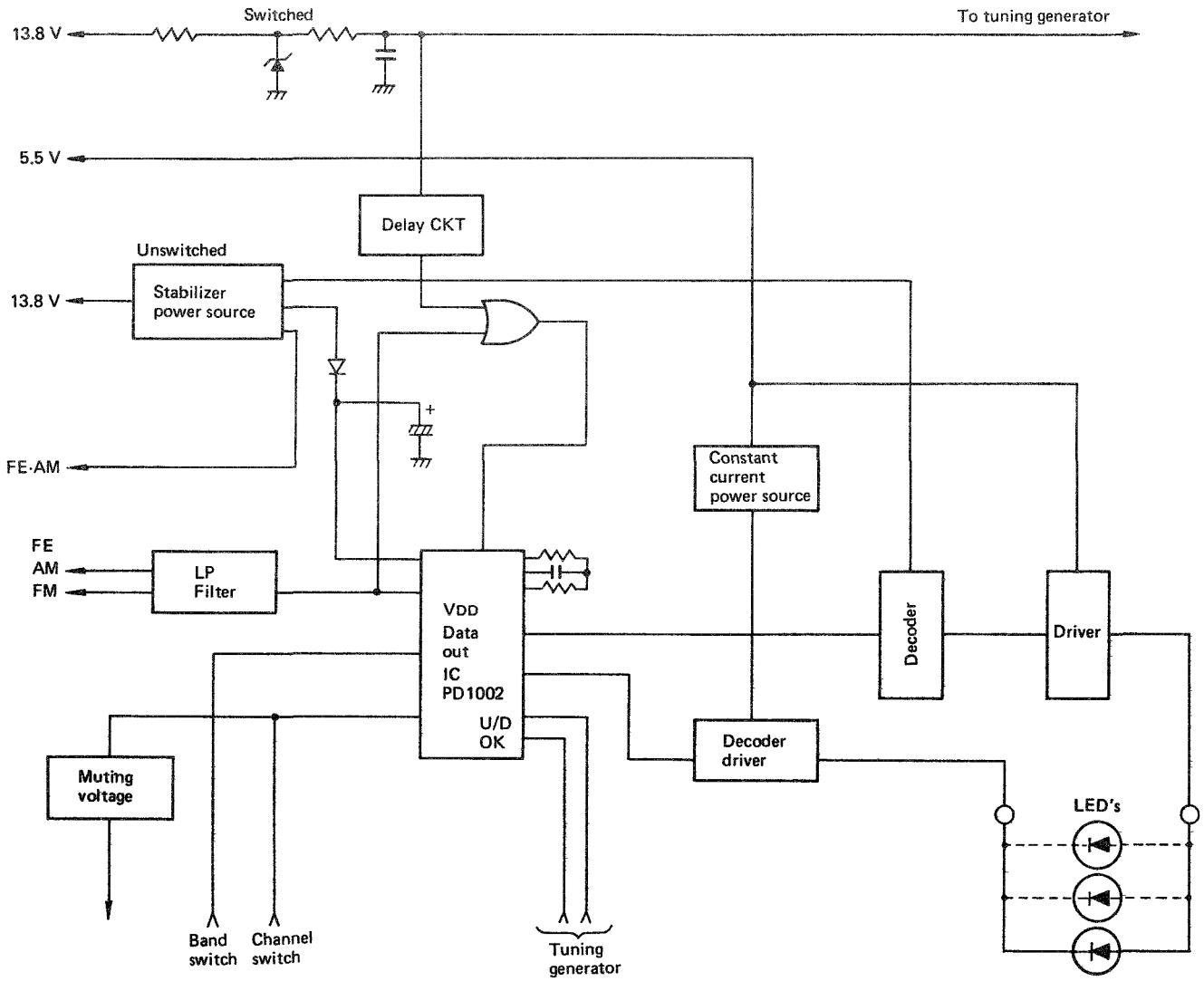


Fig. 6 Control Circuit Diagram

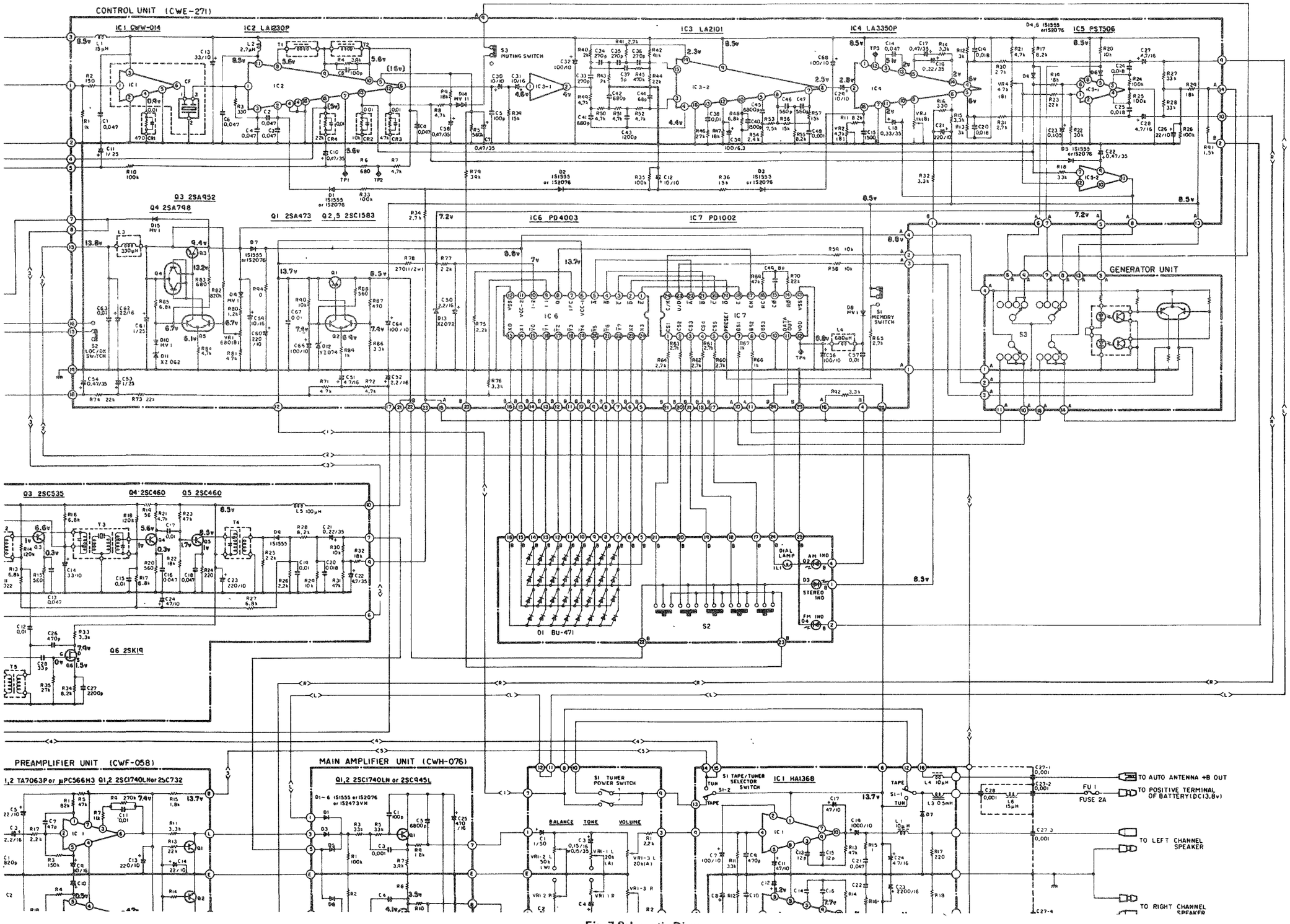


Fig. 7 Schematic Diagram

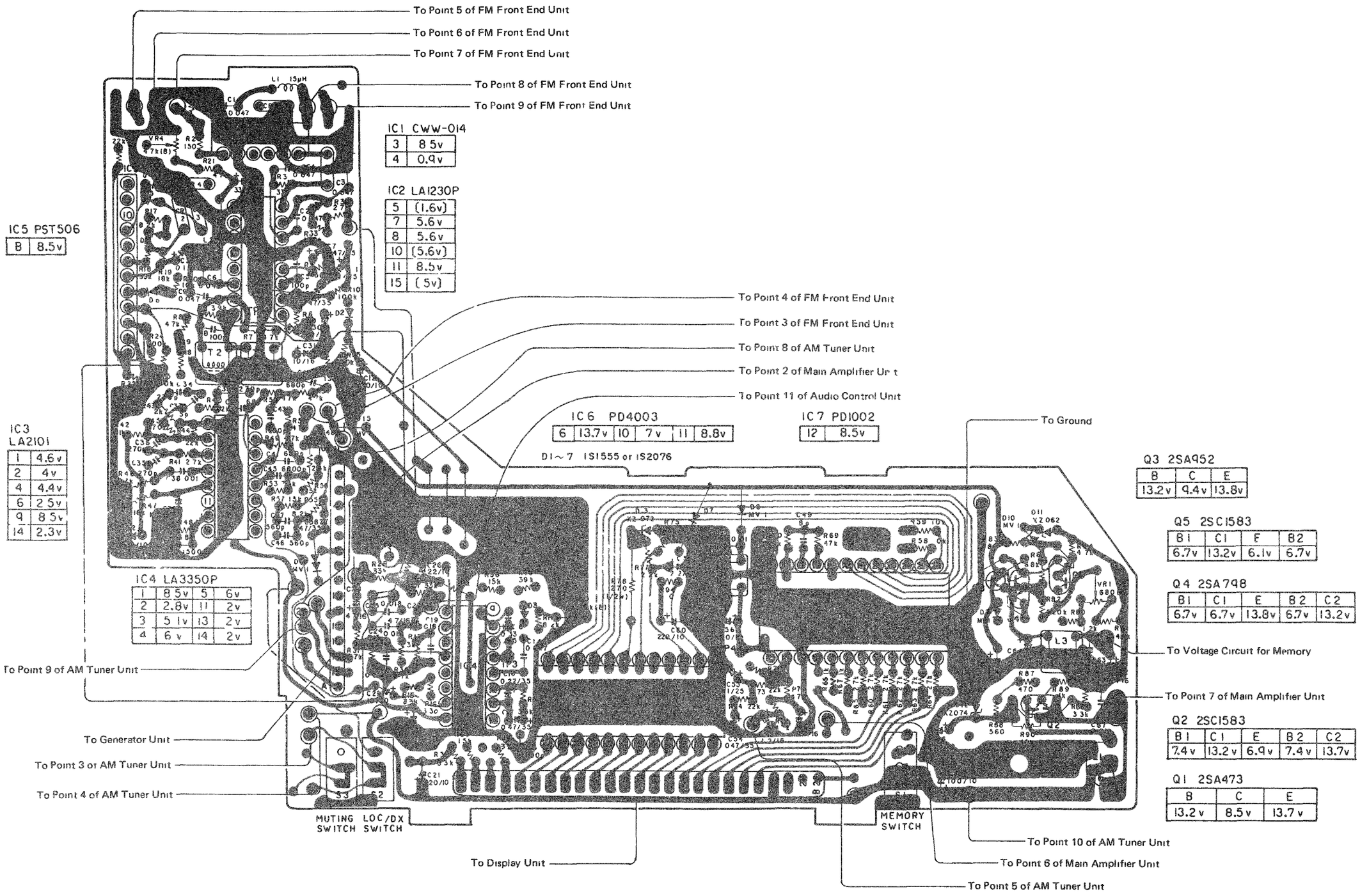
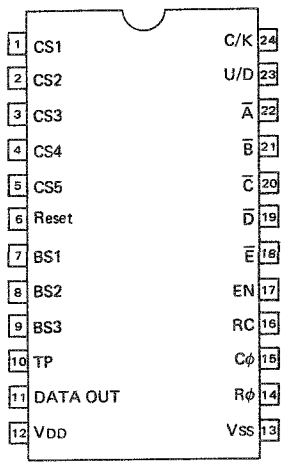


Fig. 8 Printed Circuit Board

2-2. IC PD1002

Table 2 Specifications of PD1002

Structure	Aluminum gate CMOS
Max. rating	
Max. power	15.0V
Max. power consumption	40mW
Operation temperature	−35° ~ +85°C
Storage temperature	−55° ~ +125°C
General characteristics	
Operation voltage	7.0 ~ 12.0V
Operation current	< 3.0mA
Standby period	< 0.1mA
Hysteresis gate threshold	Vp = 6.5–7.5V Vn = 2.5–3.0V
Output saturation voltage	V_{OH} > 9.9V, 0.1mA; V_{DD} = 10.0V V_{OL} < 0.1V, 0.1mA
Input frequency	< 5kHz CLK
Memory hold voltage	3.0V
Withstanding voltage against static breakdown	> 200V (200pF)
Dimensions	4.30mm x 4.35mm
Elements contained	Approximately 3,100 transistors



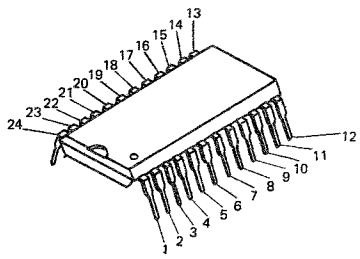


Fig. 9 IC pins alignment of PD1002

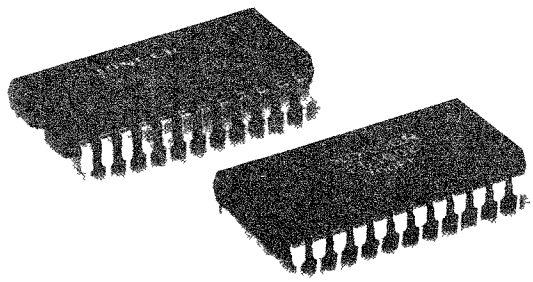


Photo 5 PD1002

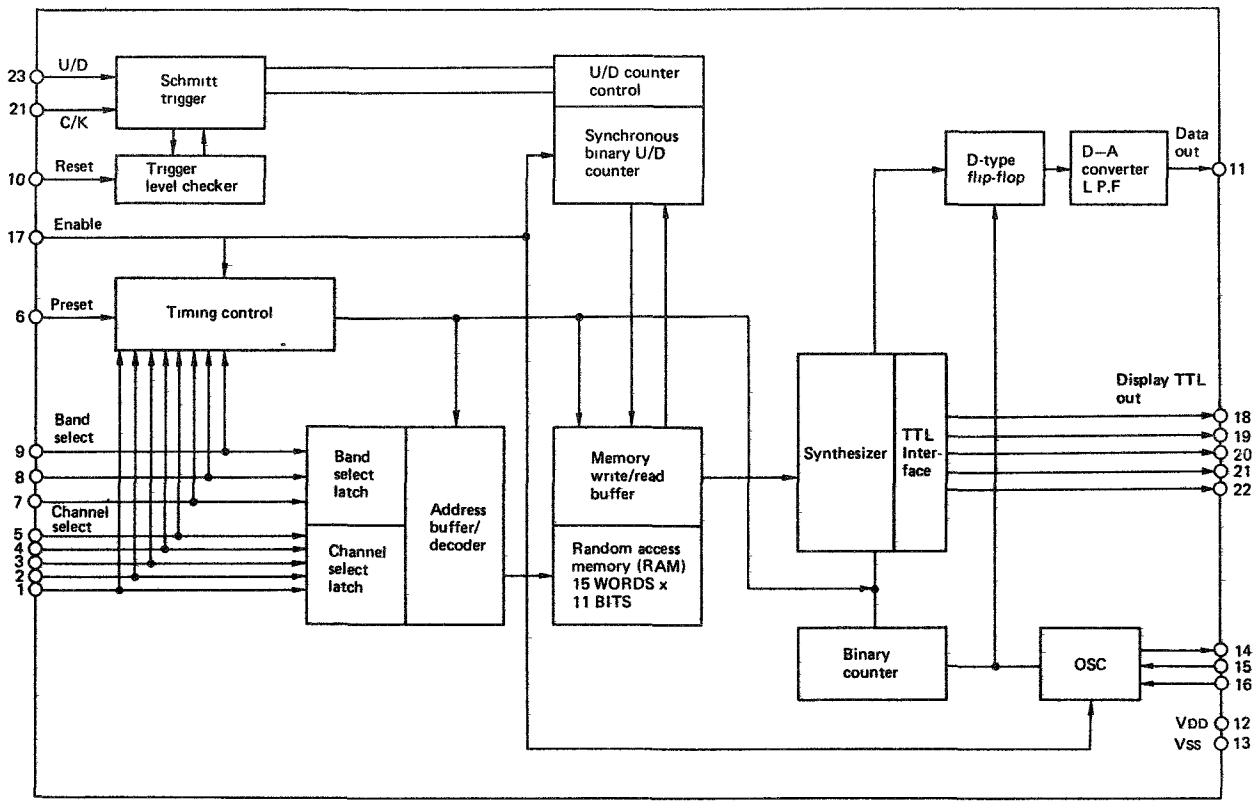


Fig. 10 PD1002 Block Diagram

3. Circuit Functions

3-1. Binary Counter

By now, you have acquired a working knowledge of the CMOS switch in the "Basic Course." Here, the flip-flop of the CMOS will be explained.

Figure 11 shows a CMOS switch. When a low-level potential pulse and high-level potential pulse are fed to G_1 and G_2, respectively, internal resistance drops, as they are P-type and N-type FET's. Electricity can travel from B to A, not only digital pulse signals, but analog signals as well can be transmitted. Therefore, it is called a bidirectional or analog switch.

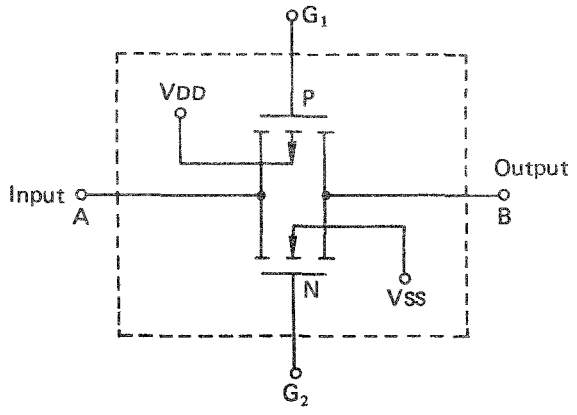


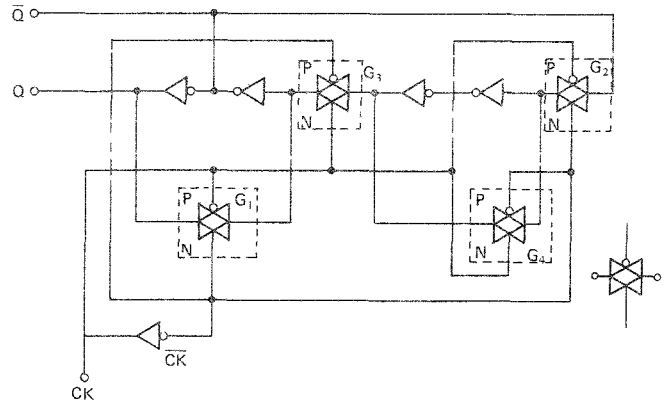
Fig. 11 FF's logic in the PD1002

In this flip-flop circuit, the CMOS switch is merely an ON/OFF switch in which the T-type flip-flop changes its ON or OFF state every time it receives an input pulse.

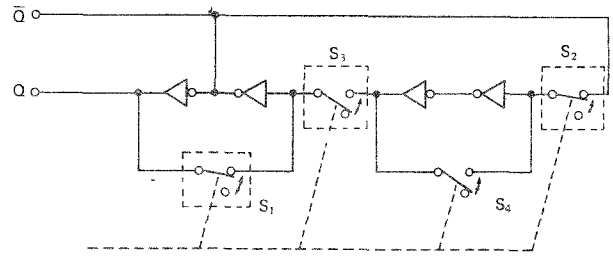
In a TTL T FF, "chattering" or a successive series of ON/OFF switching may occur during a single pulse unless the pulse width is narrow enough. But when a CMOS switch is used as a T FF, pulses from the pulse generator, though not narrow in width, can be used since the output changes state by detecting input pulse levels and not pulse edges. The time during which the state is maintained is proportional to the time of H level and level. H and L pulses having the same duration (symmetric type pulse) such as those generated by a pulse generator, are convenient.

Fig. 12 shows part of the FF's logic within the PD1002. In Fig. 12 (b), the four switches are complementing each other. The present input state is L when there is no pulse at C/K. If a pulse is fed to C/K, it is then inverted. The gate action variations depend on pulse polarization which are as follows:

(a) Logic diagram CMOS T-FF



(b) CMOS SW's relation



(c) Timing chart

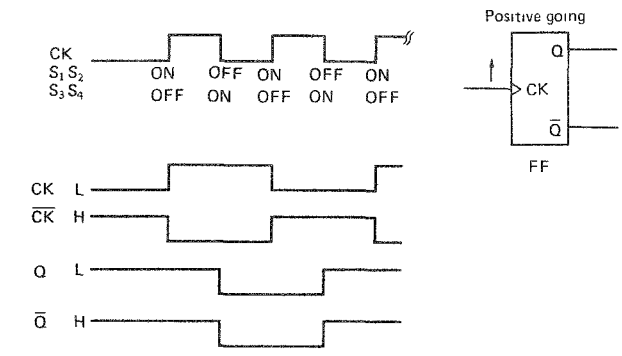


Fig. 12 Binary counter flip-flop

Table 3 Gates' Action

	G_1	G_2	G_3	G_4
P input	L	L	H	H
N input	H	H	L	L
Action	ON	ON	OFF	OFF

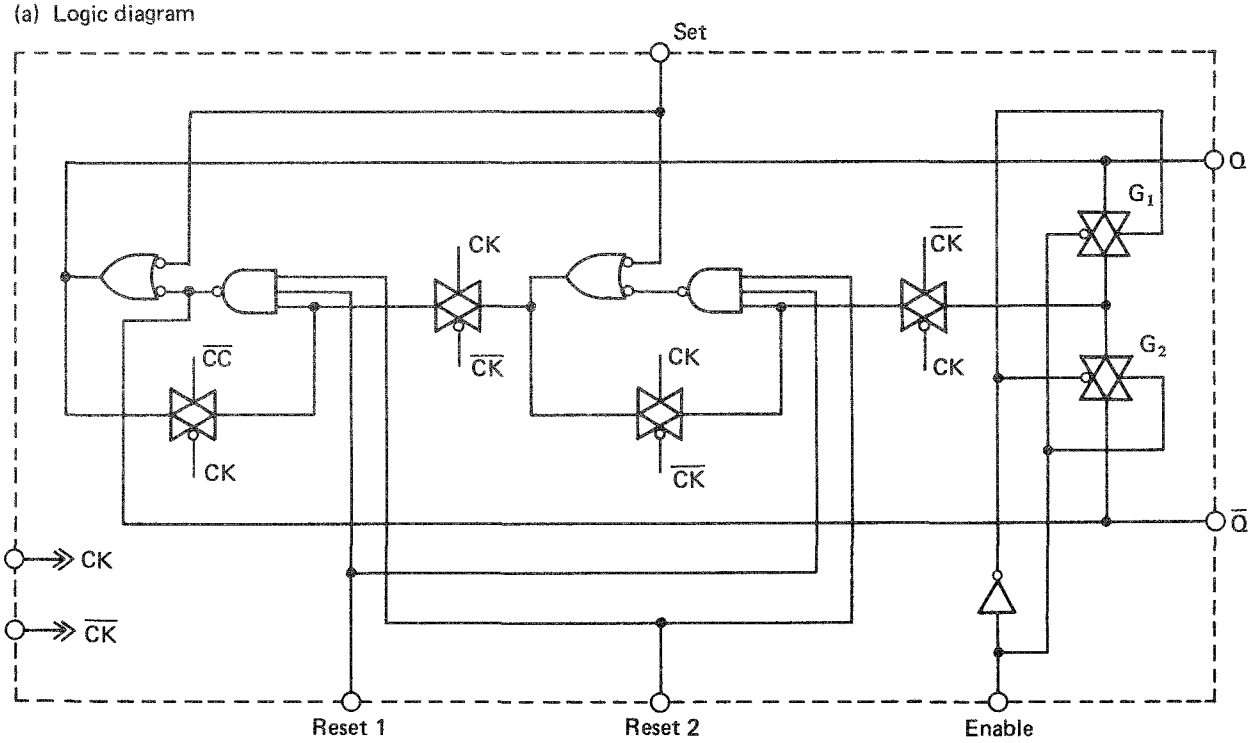
Therefore, L-level pulses appear at $\bar{Q}$, and H-level at Q. When a pulse is fed, the C/K level becomes H and the output state reverses. A binary counter composed of 11 FF's connected in series is inside the IC and can count up to 2048 pulses. Refer to Fig. 17.

3-2. Binary Up/Down Counter

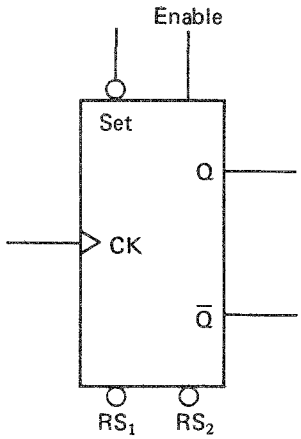
As explained in the "Basic Course," an Up counter is a binary counter whose primary stage FF's output Q is connected to the next FF's C/K input. In this way, the count increases in proportion to the number of pulses fed into the input stage. With a Down counter, the output is $\overline{Q}$ instead of Q, which is also connected to the next FF.

The Up/Down counter judges the direction of the tuning knob's rotation from the relationship between the rise times and levels of two pulses, then switches the output to Q or $\overline{Q}$, which in turn causes an increase or decrease in the count in order to obtain a count corresponding to the frequency of the desired station (Refer to the "Basid Course" on Counters).

(a) Logic diagram



(b) FF operation



S	RS_1	RS_2	U	D	Q	$\overline{Q}$
–	0	–	–	–	–	0
0	1	1	–	–	1	0
1	1	0	–	–	0	1

$S = RS_1 = RS_2 = 1$

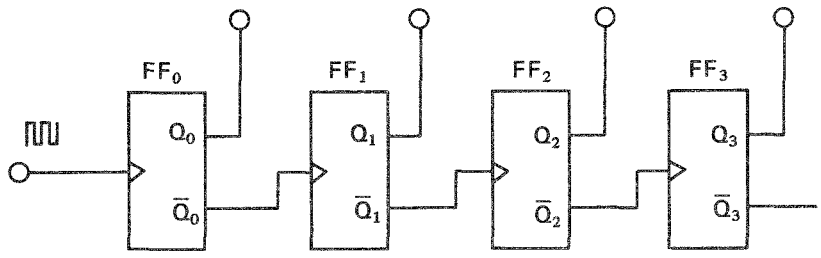
Function table

CK	EN	G_1	G_2	Qn+1
↑	1	OFF	ON	$\overline{Q}n$
	0	ON	OFF	$\overline{Q}n$

Fig. 13 U/D counter flip-flop

The C/K pulse and U/D pulse are fed to pins 22 and 23 of the IC (PD1002). The U/D pulse is then fed to the ENABLE terminal to control G_1 and G_2, and switches FF's outputs (Q and $\overline{Q}$).

(a) Binary counter



(b) Output waveform

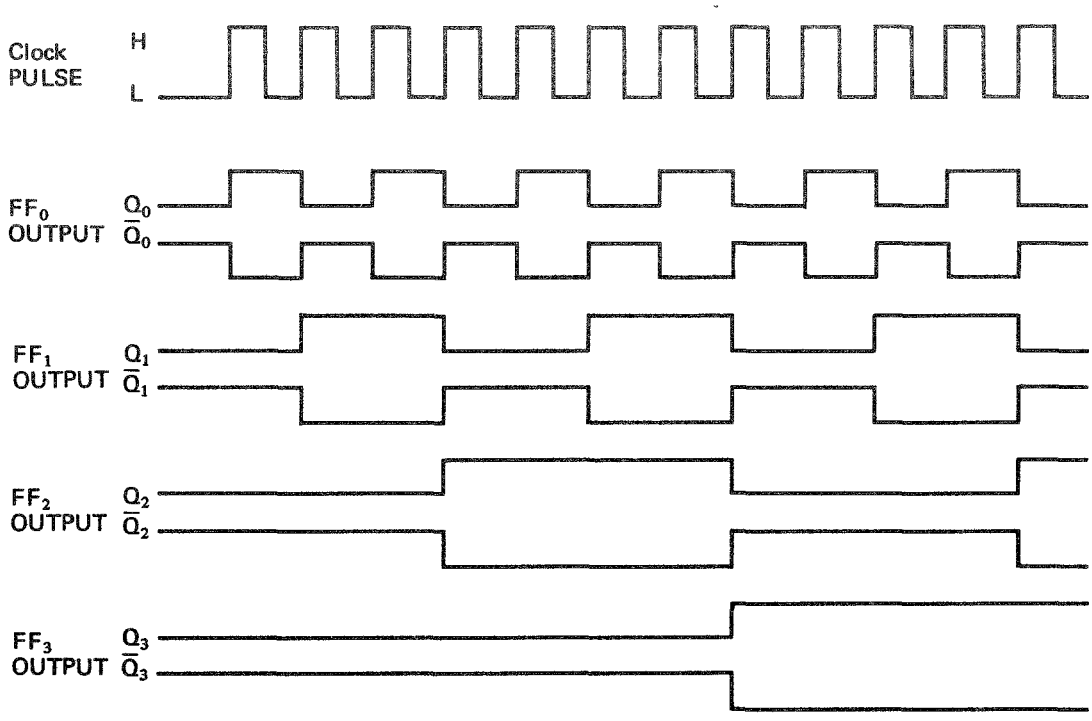


Fig. 14 Binary counter and its output waveform

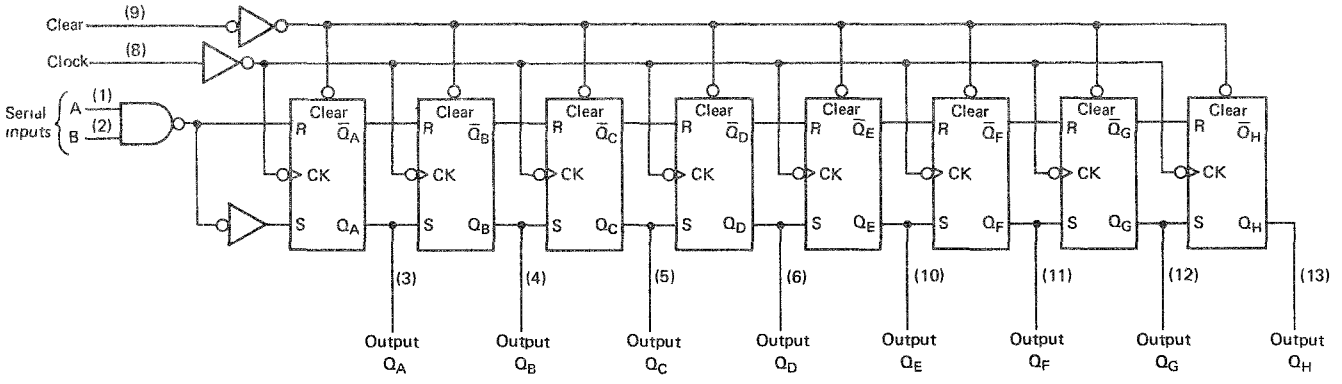
3-3. Memory Buffer (Shift Register)

The memory buffer circuit is called the shift register and is located between the counter and the memory cell block. Flip-flops were discussed briefly in the "Basic Course" and can be considered as a kind of memory device which can hold a state from the time a pulse is fed to the clock input until the next pulse is fed in. It neither counts pulses nor adds or subtracts. Then why is it so important? Because it enables parallel transfer of data and data output without affecting preceding stages.

There are two methods of transmitting data (numbers) from one circuit to another, serial and parallel transmission [Fig. 15(a) and Fig. 15(b)]. We will describe their functions with the use of two binary counters for a clearer understanding.

In serial transfer, two counters are connected in series so that the output of one counter is fed to the other counter's input. In this way, data can be transferred to each FF in succession through a single route (channel). However, in serial transfer, the transfer of information takes time, according to the amount or length of the data to be transmitted.

(a) Serial transfer



(b) Serial/parallel transfer

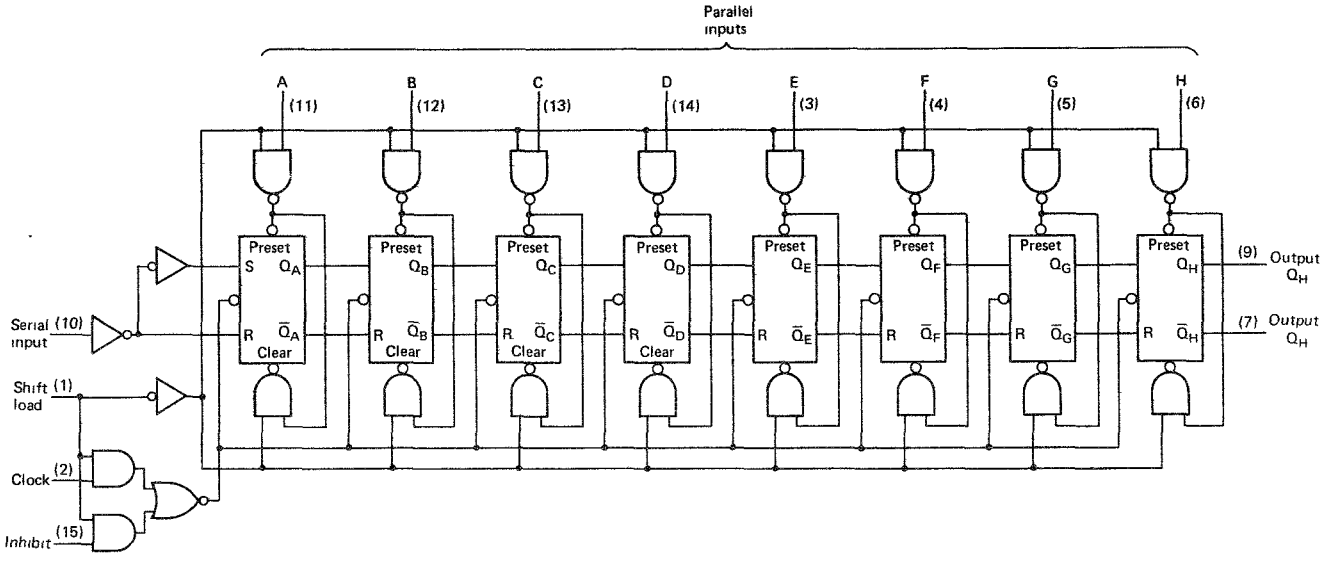


Fig. 15

In parallel transfer, two counters are connected in parallel so that data is transferred, by a pulse, to each FF simultaneously. In this way, data of a fixed length (a six-digit number for example) can be transfered into a memory unit quickly.

Fig. 15 (b) shows an example of a serial/parallel input-type register. A register plays the following three roles:

1. Writing of memory
2. Reading of memory
3. Providing output to a voltage synthesizer as a memory buffer

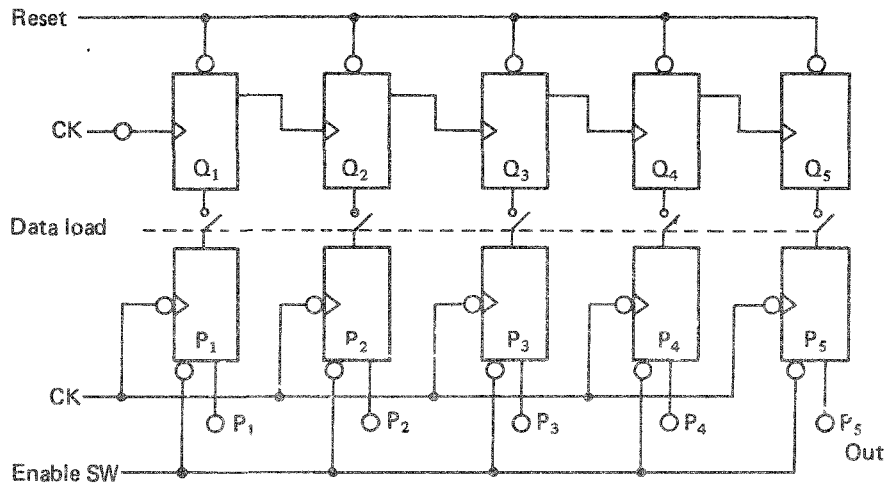


Fig. 16 Principle of parallel data transfer

3-4. Memory Read/Write

The memory tuning portion of the KE-2000 (KE-2300) consists of a memory cell which contains 15 storage units. Each unit is composed of 11 FF's (11 bits = 2048). To store and recall data, each memory unit is assigned with an address code, a total of 15 (See Table 4). To store five stations for each waveband (AM, FM and LW), 15 memory units are required–five for AM, five for FM and five for LW. Refer to Fig. 10.

A1	F00 10	F00 9	F00 8	F00 7	F00 6	F00 5	....		F00 0
A2	F01 10	F01 9	F01 8	F01 7	F01 6	F01 5	....		F01 0
A3	F02 10								
A4	F03 10								
A5	F04 10								
A6	F05 10								
A7	F06 10								
A8	F07 10								
A9	F08 10								
A10	F09 10								
A11	F11 10								
A12	F12 10								
A13	F13 10								
A14	F14 10								
A15	F15 10								

Table 4 Location of 2048 memory cell

Storing a station (writing) in a memory unit is done by pressing the MEMORY (Write Switch) and the PRESET (Address Switch) buttons simultaneously (Fig. 18). When this occurs, data (the turned station) is transferred from the shift register to the FF's for storage. Data can be recalled from the memory buffer by depressing the PRESET button, which turns the LOAD and ADDRESS switches on simultaneously. This memory can be referred to as a Random Access Memory (RAM) as writing and reading can be done freely.

Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}
1	2	4	8	16	32	64	128	256	512	1024

Table 5 FF storage unit for Preset Memory and binary mount conversion

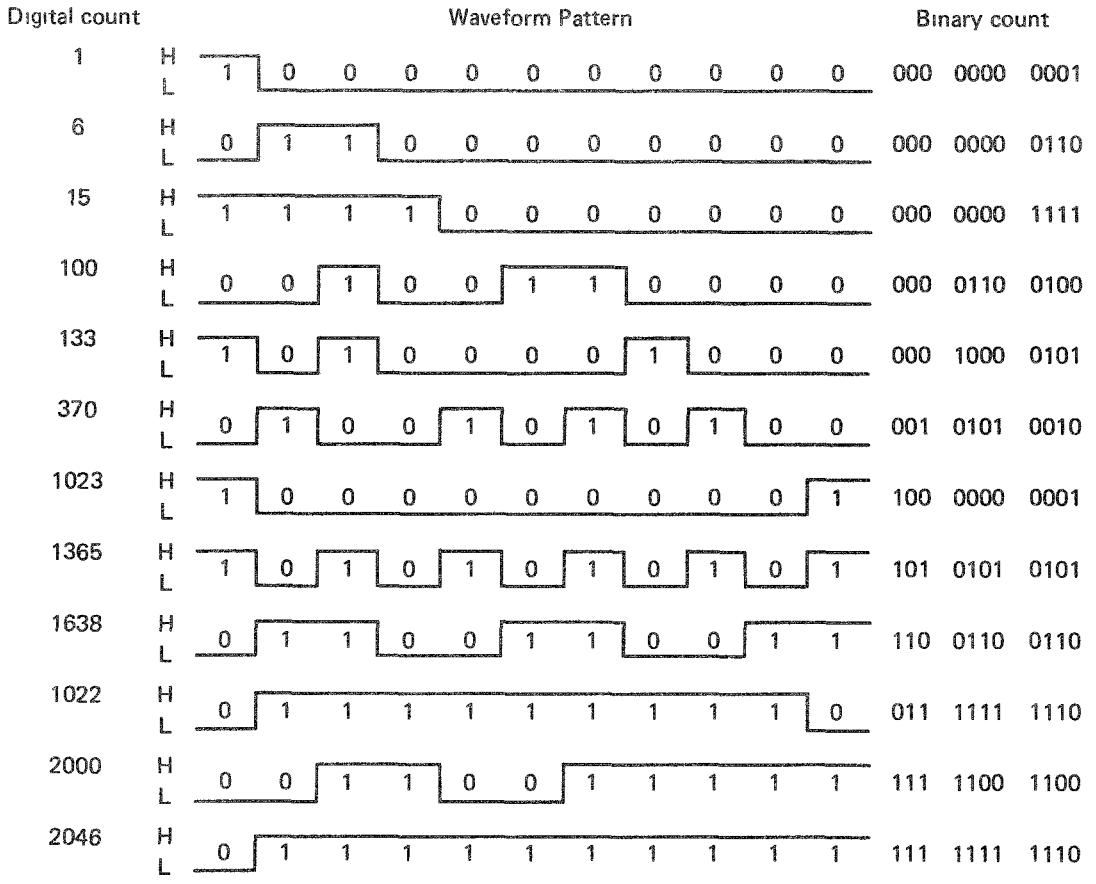


Fig. 17 Pulse pattern of binary counter
(Pulse patterns in the binary counter's shift register and memory cell)

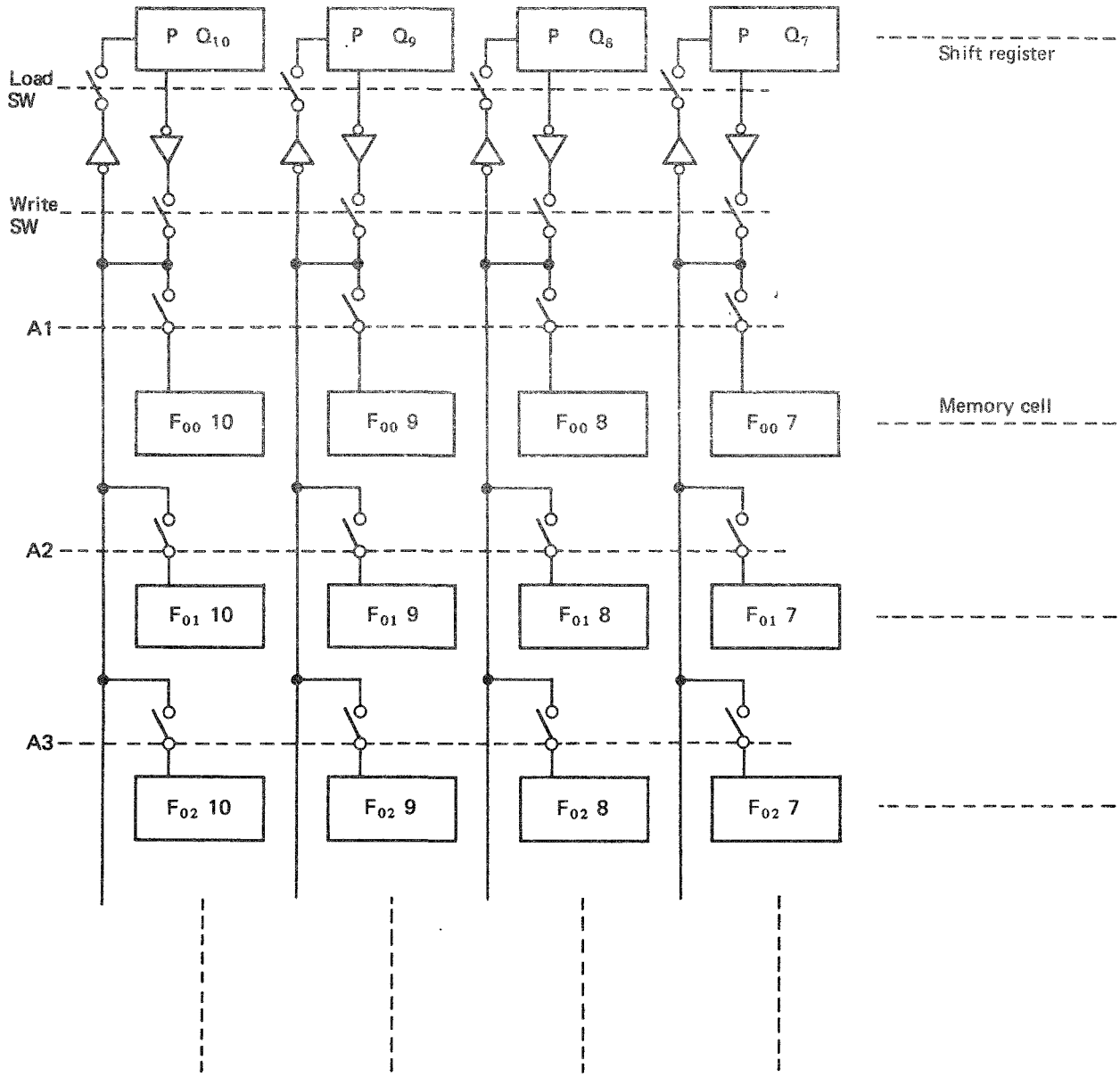


Fig. 18 Memory read/write section

Connection of the shift register and memory address (up to 15). Data is stored in the memory by operating the WRITE and LOAD switches.

3-5. Pulse Synthesizer

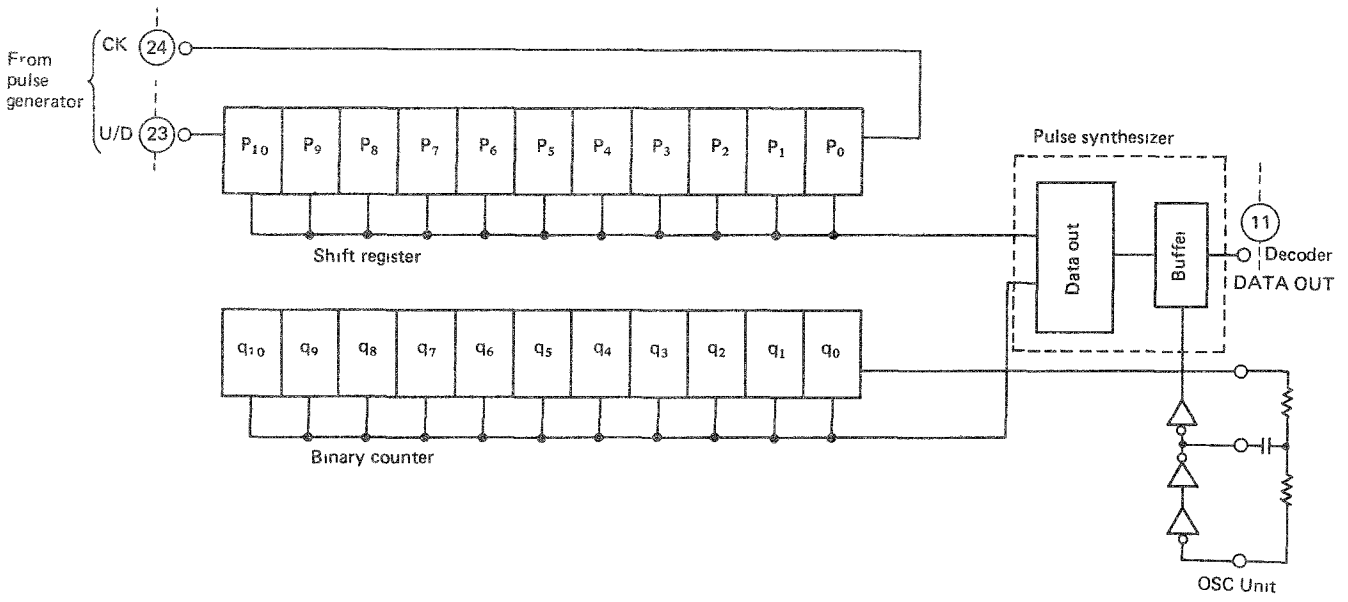


Fig. 19 Pulse Synthesizer Block Diagram

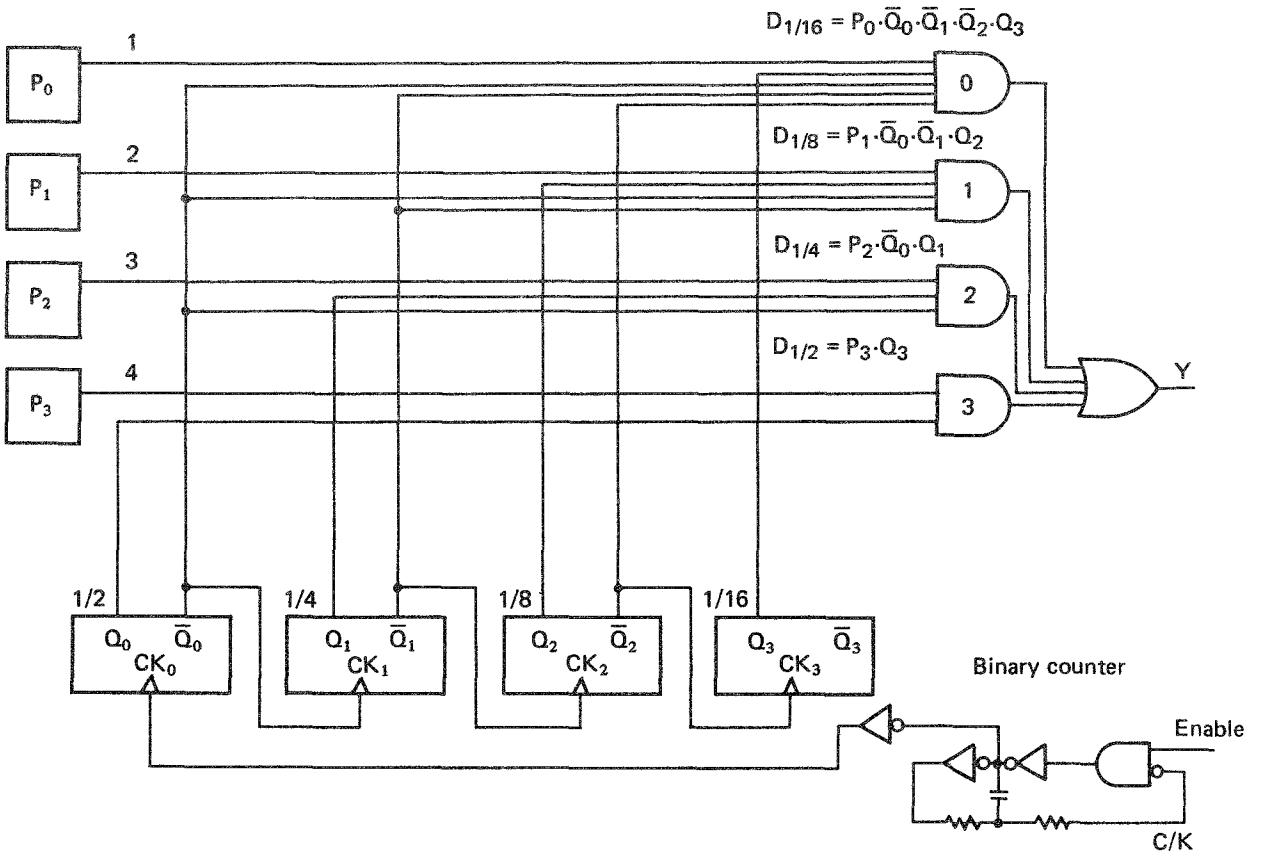


Fig. 20 Pulse Synthesizer Logic Diagram (4-bit)

Fig. 19 is a simplified schematic of the synthesizer. Fig. 20 is a detailed figure of a four-bit synthesizer. As explained earlier, pulses generated by the oscillation circuit are divided into 2,048 (stations) by 11 stages of FF's. These pulses are then fed to 2,048 counters with a cycling time of approximately 2mS. As shown in Figure 20, when all the preceding gates are H, the AND gates (four) and OR gate pulses (1MHz) are fed directly into the data out's buffer (D FF) (refer to Fig. 10). What is important here is that CK_0, CK_1, CK_2, and CK_3 face P_3, P_2, P_1 and P_0 respectively so that data is stored in the correct numerical sequence to prevent misreading. This can be expressed in a logic formula as shown on the right.

The synthesizer thus determines the period of time in which the gates must be kept open to put out pulse data (Fig. 21).

Pulse Synthesizer's logic formula

$$
\begin{aligned}
Y = {} & O_0 + O_1 + O_2 + O_3 + O_4 + O_5 + O_6 + O_7 + O_8 + O_9 + O_1 \\
& P_0 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot \overline{q}_5 \cdot \overline{q}_6 \cdot \overline{q}_7 \cdot \overline{q}_8 \cdot \overline{q}_9 \cdot q_{10} \\
& + P_1 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot \overline{q}_5 \cdot \overline{q}_6 \cdot \overline{q}_7 \cdot \overline{q}_8 \cdot q_9 \\
& + P_2 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot \overline{q}_5 \cdot \overline{q}_6 \cdot \overline{q}_7 \cdot q_8 \\
& + P_3 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot \overline{q}_5 \cdot \overline{q}_6 \cdot q_7 \\
& + P_4 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot \overline{q}_5 \cdot q_6 \\
& + P_5 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot \overline{q}_4 \cdot q_5 \\
& + P_6 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot \overline{q}_3 \cdot q_4 \\
& + P_7 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot \overline{q}_2 \cdot q_3 \\
& + P_8 \cdot \overline{q}_0 \cdot \overline{q}_1 \cdot q_2 \\
& + P_9 \cdot \overline{q}_0 \cdot q_1 \\
& + P_{10} \cdot q_0
\end{aligned}
$$

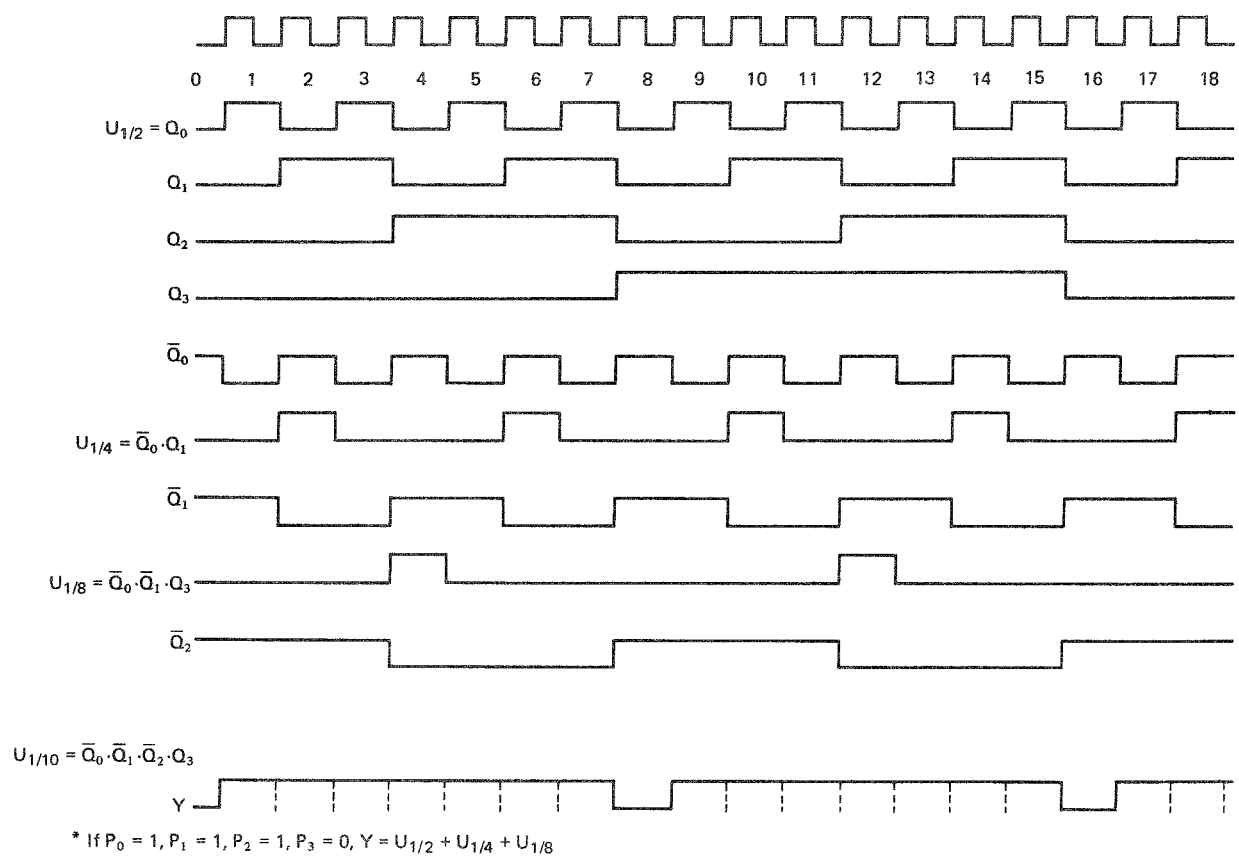
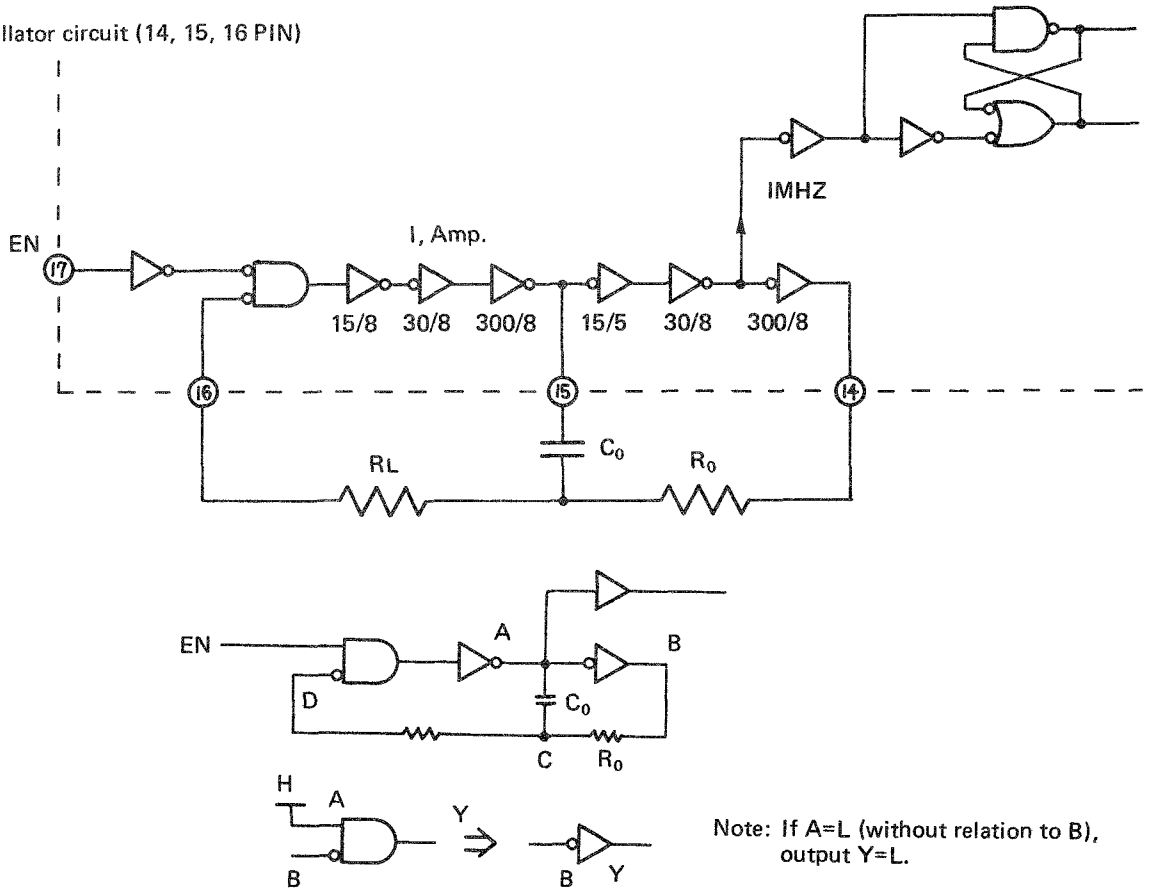


Fig. 21 Pulse Synthesizer Timing Chart

3-6. Oscillator Circuit

Pulses produced by the pulse generator and those stored in the shift register (memory buffer) cannot produce sufficient DC voltage to be supplied to the varicap in the front-end. To provide the varicap with the necessary DC voltage for frequency tuning, a voltage synthesizer is used. The synthesizer compares the high-frequency pulse wave patterns (≒ 1MHz) generated in the oscillator circuit after they have been counted by the FF's (binary counters). Since the output voltage is limited to the supply voltage, (VDD) which in this case is 10 volts from the car battery, the circuit can't employ a conventional analog amplifier. To provide the needed DC voltage in the digital circuit, a kind of pulse-width amplifier is used.

(a) Oscillator circuit (14, 15, 16 PIN)



(b) Oscillator waveform

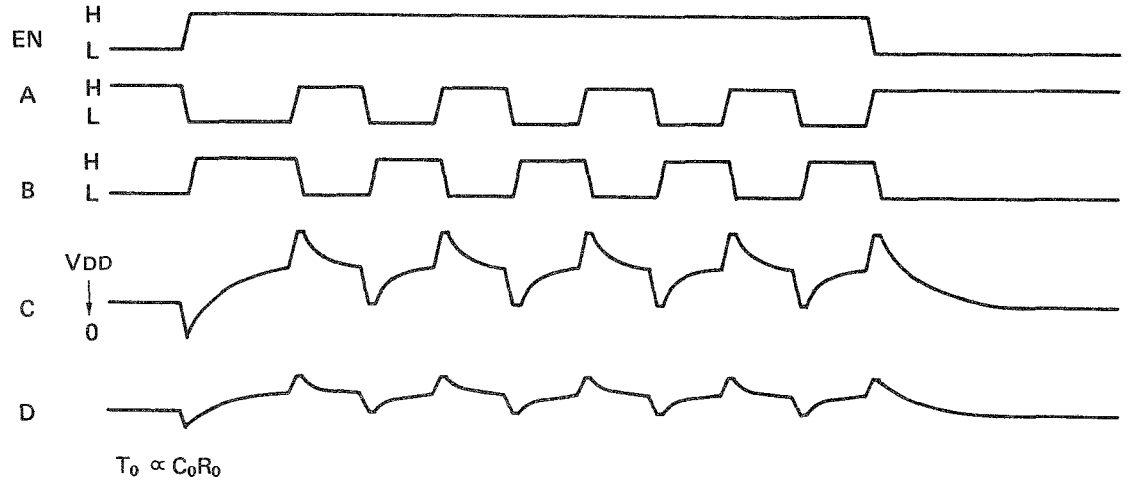


Fig. 22 Oscillator

3-7. TTL Interface

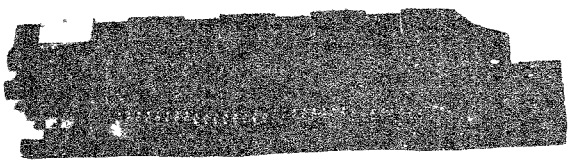
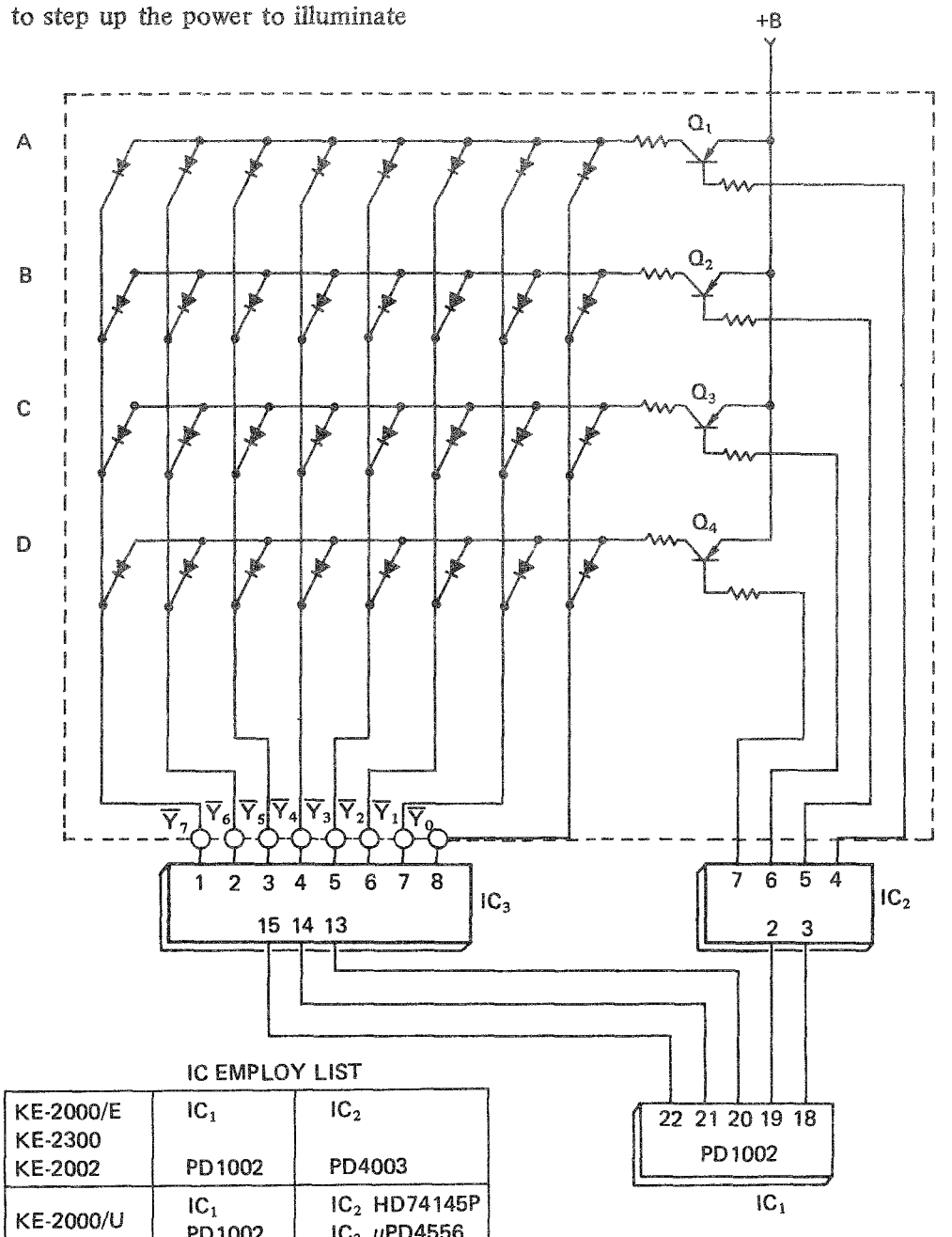


Photo 6

Unlike conventional car tuners, the KE-2000 has no tuning pointer for station indication, but instead, 32 bar LED's are used. Since the output power of the CMOS IC PD1002 is too low to drive the LED's, a TTL IC is used to step up the power to illuminate the LED's.

To drive all 32 LED's, 32 outputs are required (5 bits). Voltage appears at pins 18 ($\overline{E}$), 19 ($\overline{D}$), 20 ($\overline{C}$), 21 ($\overline{B}$) and 22 ($\overline{A}$) respectively, in accordance with the tuning frequency (Refer to Table 1). The LED's are connected to a matrix circuit, when a signal is received, outputs A, B and C of PD1002 are fed to IC_3 (3 bits) and D and E to IC_2 (2 bits). With this combination, the circuit can drive the LED's from 1 to 32.



IC EMPLOY LIST

KE-2000/E KE-2300 KE-2002	IC_1 PD1002	IC_2 PD4003
KE-2000/U	IC_1 PD1002	IC_2 HD74145P IC_3 μPD4556

Fig. 23 KE-2000/U LED TUNING DISPLAY UNIT

Fig. 23 shows the LED tuning display matrix. In the figure, eight pins of 3-bit IC_1 and four pins of 2-bit IC_2 are used. A total of 32 (4x8) combinations of input pulses form the AND matrix. As IC_1 is negative logic input, it operates when L-level pulses are received, while H-level pulses are required for IC_3, which is positive logic.

When L-level pulses are fed from IC_2, $Q_1 \sim Q_4$ become ON and the collector's level becomes high. When $\overline{Y}_1 \sim \overline{Y}_2$ become low, the cathode of the LED will become low and electricity will flow to light the LED's.

Recently manufactured KE-2000 series models all use PD4003. It is actually a combination of IC_1 and IC_3 but its theory of operation is the same. Fig. 24 shows the internal circuit of PD4003.

Tuning pointer	E	D	C	B	A	IC_1	IC_3
0	0	0	0	0	0	1	a
1	0	0	0	0	1	2	a
2	0	0	0	1	0	3	a
3	0	0	0	1	1	4	a
•	•	•	•	•	•	•	•
7	0	0	1	1	1	8	a
8	0	1	0	0	0	1	b
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
31	1	1	1	1	1	8	d

Table 6 NO & Matrix Operation of LED

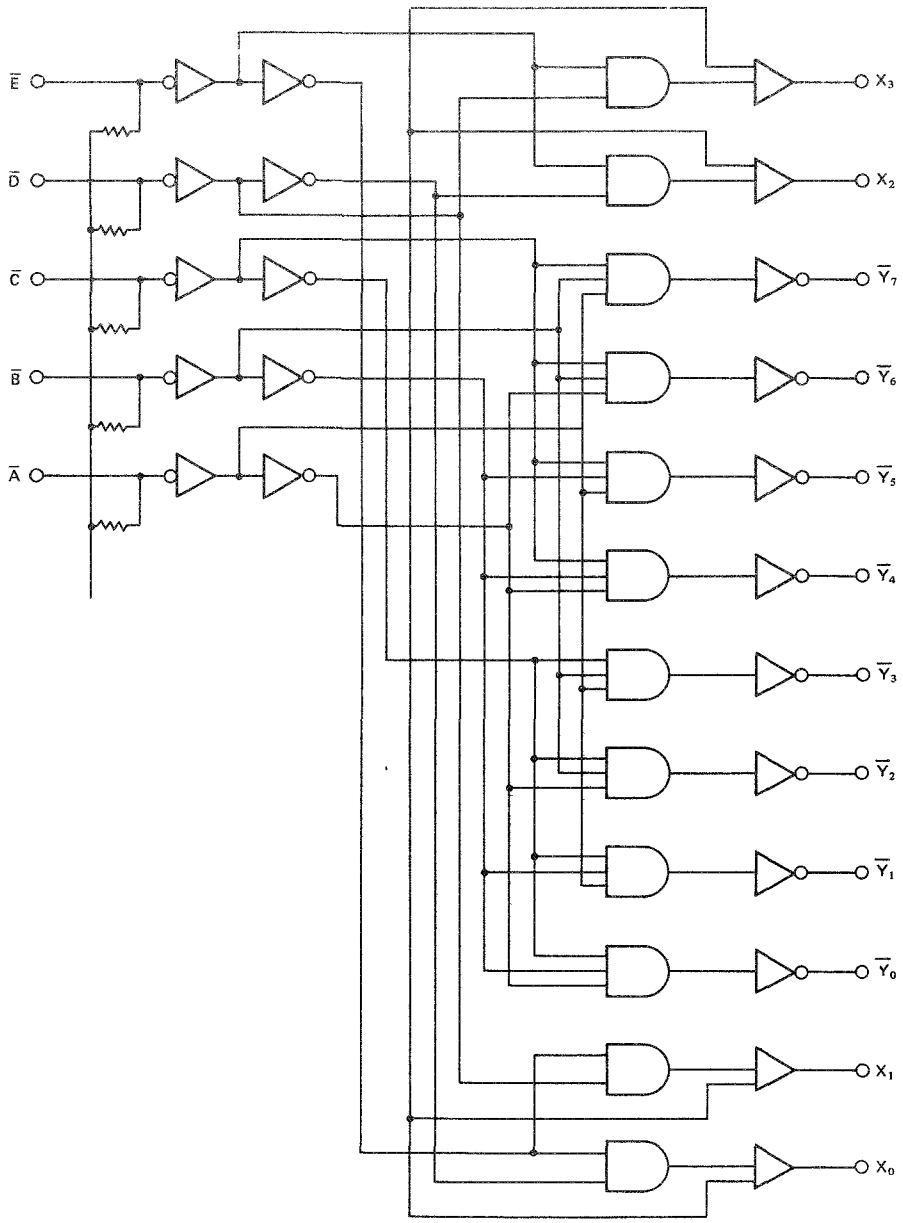


Fig. 24 BLOCK DIAGRAM OF PD4003

3-8. Generation of Tuning Voltage and Filter Circuit

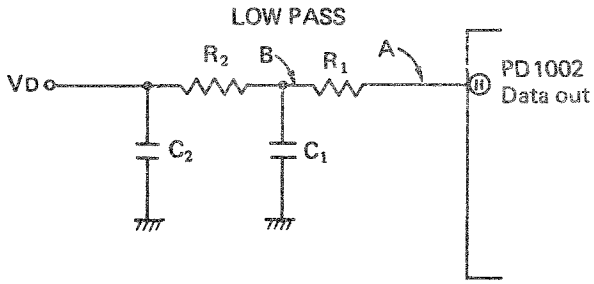
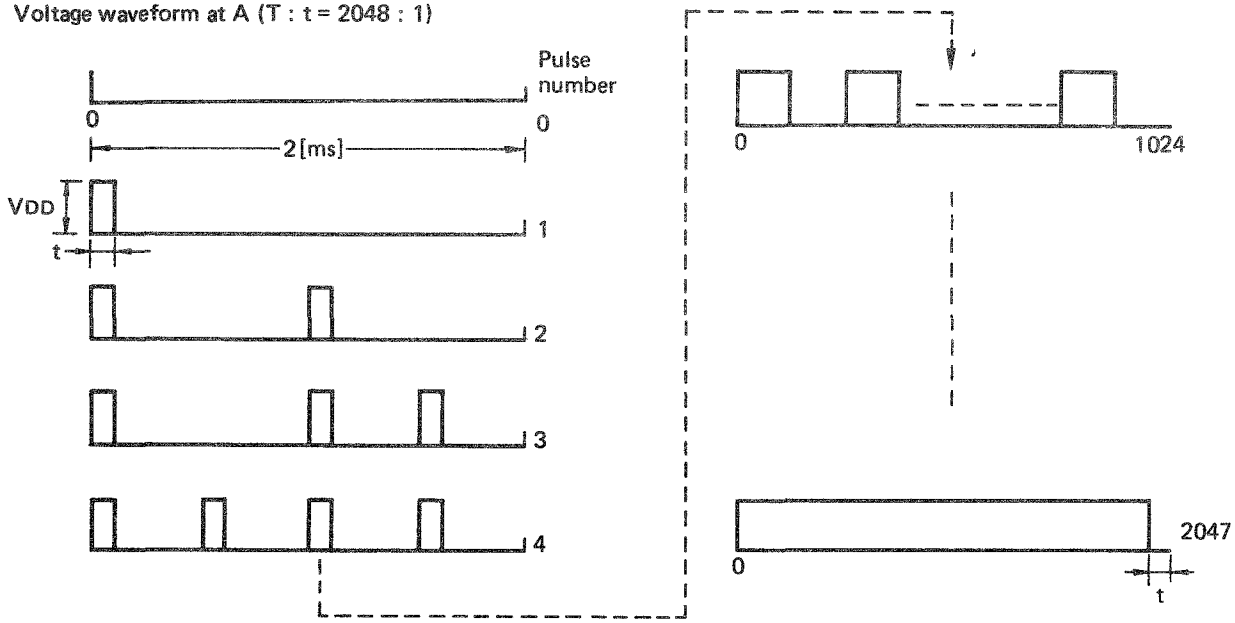


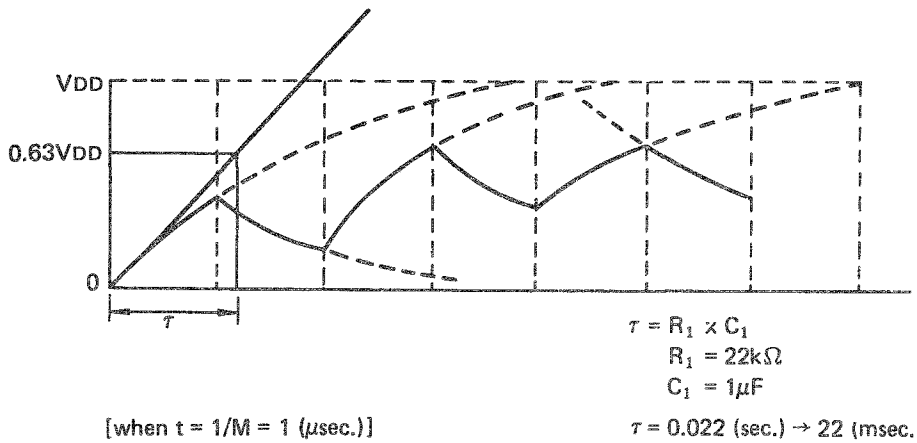
Fig. 25

As output from DATA OUT is in the form of a pulse, it must be converted from digital to analog. To this end, a low-pass filter is required (Fig. 25). C_1 is charged through R_1. The product of R_1 x C_1 is 0.022 (sec) ~ 22 (msec.). Even when 2048 pulses are chrged in C_1, good linearity of the AC-DC converter can be achieved. In addition, the pulses are flattened further by R_2 and C_2 and can be considered as DC at the output.

(a) Voltage waveform at A (T : t = 2048 : 1)



(b) Voltage waveform at B (at 1024)



[when t = 1/M = 1 (μsec.)]

Fig. 26 Voltage waveforms at A and B

Thus DC voltage corresponding to the number of pulses can be generated to change the tuning frequency by the varicap.

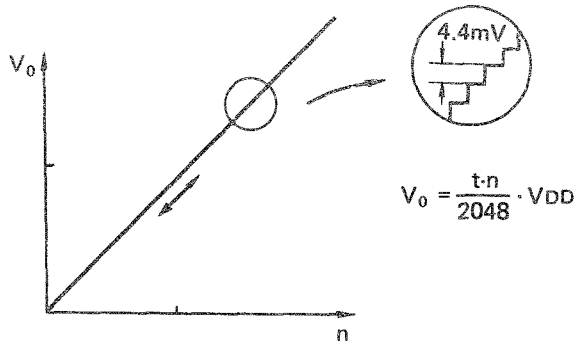


Fig. 27

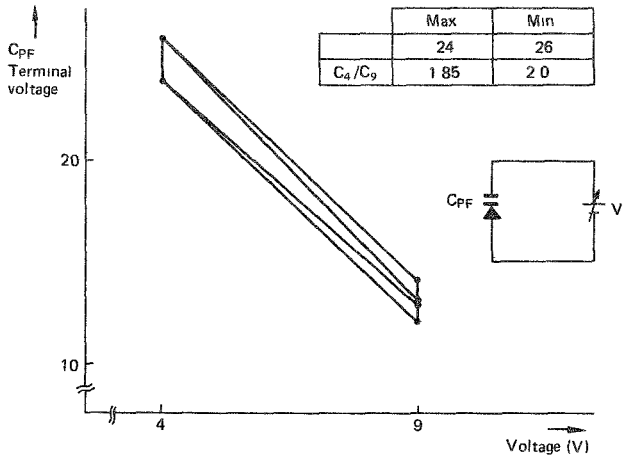


Fig. 28 ITT 310A (varicap) characteristics for FM

3-9. Troubleshooting

There are two or three IC's used in the digital circuitry of the KE-2000. In order to simplify and speed up servicing, it is necessary to understand the functions of each one.

Fig. 29 is a block diagram outlining the circuits surrounding both IC's and their connections within the circuits. With the aid of this diagram you can locate problems in the circuit by following the procedures outlined in this section.

a) FM tuner does not function.

Check to see if the voltage of the power source in the FM front-end and FM IF circuit is normal. If normal, measure the DC voltage from the filter-out to the front-end (0 ~ 8V). If you find nothing wrong with the voltage, then the trouble may be in the front-end. If not, check to see if PD1002 is alright. If the voltages at every terminal are normal, then check the pulse generator.

b) LED's do not light.

First measure the voltage fed to the LED's. If normal, check the voltage of TTL IC's power source and then the input and output voltages of that TTL IC. If you still find nothing wrong, check PD1002 (Refer to TTL Interface).

c) LED tuning indicators do not move.

Check if the pulse generator is alright and then check the soldered leads of the photo coupler. If you find nothing wrong, then check PD1002.

These are some of the troubleshooting procedures you can perform with the aid of the diagram. Since most of KE-2000's functions are centered around the CMOS PD1002, whose susceptibility to heat and static electricity is far gerater than that of TTL IC's, the trouble, in most cases, will involve PD1002. If replacement of PD1002 becomes necessary, make sure you use a well heated soldering iron and be sure to ground it to earth. Replace the damaged CMOS as quickly as possible to prevent prolonged exposure to heat. To facilitate the removal of the IC from the circuit board, we suggest the use of desoldering tools (featured in photo).

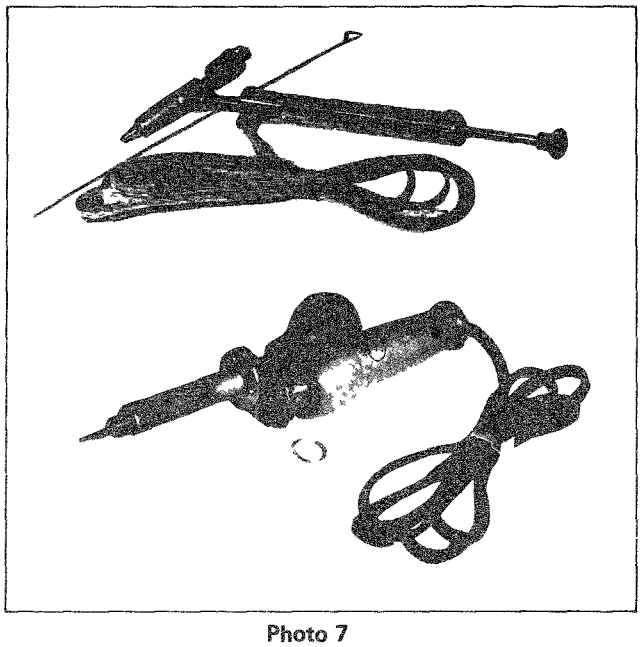


Photo 7

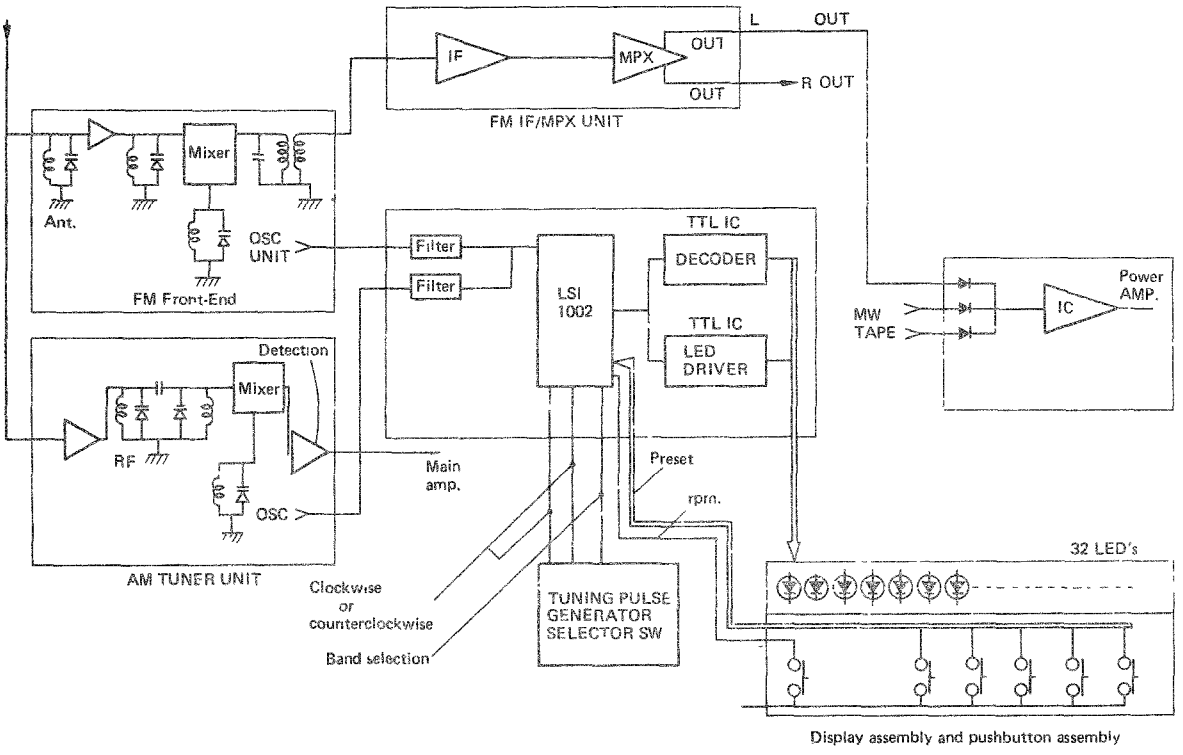


Fig. 29 KE-2000 Block Diagram

Boolean Algebra

1. Boolean algebra

Boolean algebra is like toy building blocks. Such blocks, unlike ordinary wooden blocks, have rules of connection which enable you to build or construct something.

Boolean algebra, too, has rules. By adhering to these rules, very complicated construction and problem solving can be done. Don't be fooled by the strange name, just imagine that you are actually building with toy blocks.

Boolean algebra, also called logical algebra or transformation algebra, was originated by George Boole (1815~1864). It was originally invented to make logic mathematical. But now, about 100 years later, it is frequently used in logic design of digital circuits.

2. Boolean operations

There are only three operations in Boolean algebra– that is, addition, multiplication and negation, no subtraction nor division. Let's start with addition. Under the Boolean operation, addition is referred to as logical sum which is quite different from ordinary addition. See Fig. 1.

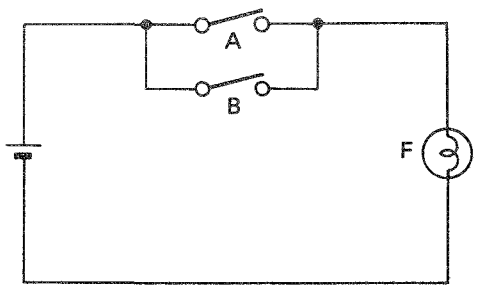


Fig. 1 OR circuit

Here, assume the following:

Switch A is closed: A = 1
Switch A is open: A = 0
Switch B is closed: B = 1
Switch B is open: B = 0
Lamp is on: F = 1
Lamp is off: F = 0

A	B	F = A+B
1	1	1
1	0	1
0	1	1
0	0	0

Table 1: Truth table of NOR circuit

As the figure shows, the lamp will be on when switch A is closed or when switch B is closed. This or relationship is called logical sum or OR. Logical sum is represented by the symbols A + B, which is read "A or B." It symbolizes the operation of the OR gate itself (actually, the symbol was in existence when the gate was produced).

Next, multiplication. It is called logical multiplication. In the lamp circuit shown in Fig. 2, switches A and B must be closed to switch on the lamp. This and relationship is called logical multiplication or AND.

This is symbolized by A·B, which is read "A and B." Like OR, the AND gate's operation represents the AND relationship itself.

Finally, negation. This is the easiest of the three. It is a relationship where F is 0 when A is 1, and 1 when A is 0. This is represented by $\bar{A}$, which is read "not A."

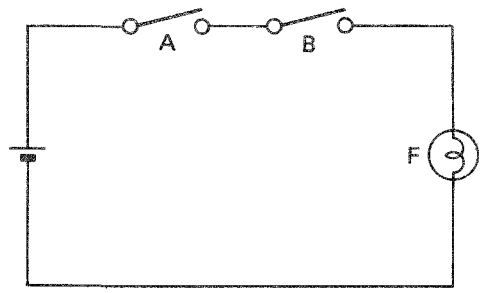


Fig. 2 AND circuit

A	B	F = A·B
1	1	1
1	0	0
0	1	0
0	0	0

Table 2: Truth table of AND circuit

A	F = $\bar{A}$
1	0
0	1

Table 3: Truth table of NOT circuit

3. Basic nature of Boolean algebra

Now that you have an overview of Boolean operations, you are now ready to learn how to combine these basic operations as in logic designing, but first, let's study the basic nature of Boolean algebra.

Nature	Formula
Nature 1: Law of Involution	$\bar{\bar{A}} = A$
Nature 2: Independent Law	$A \cdot A = A$, $A+A = A$
Nature 3: Commutative Law	$A \cdot B = B \cdot A$, $A+B = B+A$
Nature 4: Associative Law	$(A \cdot B) \cdot C = A \cdot (B \cdot C)$ $(A+B)+C = A+(B+C)$
Nature 5: Distributive Law	$A \cdot (B+C) = A B + A \cdot C$ $A+B \cdot C = (A+B) \cdot (A+C)$
Nature 6: Law of Absorption	$A \cdot (A+B) = A$, $A+A \cdot B = A$
Nature 7: De Morgan's Theorem	$\overline{A \cdot B} = \bar{A}+\bar{B}$, $\overline{A+B} = \bar{A} \cdot \bar{B}$
Nature 8. Law of Complementary	$A \cdot \bar{A} = 0$, $A+\bar{A} = 1$
Nature 9: Unit Element Law	$A \cdot 1 = A$, $A+0 = A$
Nature 10.	$A \cdot 0 = 0$, $A+1 = 1$
Nature 11:	$\bar{1} = 0$, $\bar{0} = 1$

Table 4: Basic nature of Boolean algebra

Table 4 shows 11 basic laws. First, you have to understand them well—some are easy and others are a little more difficult.

- **Nature 1: Law of Involution** $\bar{\bar{A}} = A$

This means that the negation of A's negation is A itself, just as if nothing had been done to it. The truth table is shown in Table 5.

A	$\bar{A}$	$\bar{\bar{A}}$
1	0	1
0	1	0

Table 5: Truth table of Nature 1

- **Nature 2: Independent Law**

A	A	A·A
1	1	1
0	0	0

A	A	A+A
1	1	1
0	0	0

Table 6: Truth table of Nature 2

This means that logical multiplication and logical sum of A and A is A. The relationship of A is expressed as follows:

$A \cdot A \cdot A \cdot \ldots\ldots \cdot A = A$

$A+A+A+ \ldots\ldots +A = A$

In other words, logical multiplication and logical sum of A itself are the same as if nothing has been done to it.

- **Nature 3: Commutative Law**

$A \cdot B = B \cdot A$

$A+B = B+A$

The relationship of A and B is rather simple and does not require an explanation.

- **Nature 4: Associative Law**

$(A \cdot B) \cdot C = A \cdot (C \cdot B)$

$(A+B)+C = A+(B+C)$

The logic shown in truth table 7 makes the operation of Nature 4 quite apparent.

A	B	C	A·B	(A·B)·C	B·C	A·(B·C)
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	1	1	1	1	1
1	1	0	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
0	0	1	0	0	0	0
0	0	0	0	0	0	0

Table 7: Truth table of Nature 4

- **Nature 5: Distributive Law**

$A \cdot (B+C) = A \cdot B + A \cdot C$

$A+B \cdot C = (A+B) \cdot (A+C)$

A	B	C	B+C	A·(B+C)	A·B	A·C	A·B+A·C
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	1	1	1	1	1	1
1	1	0	1	1	1	0	1
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
0	0	1	1	0	0	0	0
0	0	0	0	0	0	0	0

Table 8: Truth table of Nature 5

The first formula is the same as in the conventional four rules of arithmetic. But note that the four rules do not hold true in the second formula.

The truth table (Table 8) shows that the truth value of the left side (fifth column) of the above logic is the same as the right side's truth value (last column), thereby proving the above formulae.

● Nature 6: Law of Absorption

$A \cdot (A+B) = A$

$A+(A \cdot B) = A$

This is not included in the conventional four rules, either. This strange law can be verified by the truth table in Table 9

A	B	A+B	A·(A+B)	A·B	A+A·B
1	0	1	1	0	1
1	1	1	1	1	1
0	1	1	0	0	0
0	0	0	0	0	0

Table 9: Truth table of Nature 6

● Nature 7: De Morgan's Theorem

$\overline{A \cdot B} = \overline{A}+\overline{B}$

$\overline{A+B} = \overline{A} \cdot \overline{B}$

This is the most important and famous of all the Boolean algebra laws because its operations—addition, multiplication and negation—are all included in these formulae.

The first formula means that negation of logical multiplication equals logical sum (not logical multiplication) of negated terms. The second shows that negation of logical sum is equal to logical multiplication (not logical sum) of negated terms.

Table 10 shows the truth table of Nature 7 to verify these formulae.

A	B	$\overline{A}$	$\overline{B}$	A·B	$\overline{A \cdot B}$	$\overline{A}+\overline{B}$	A+B	$\overline{A+B}$	$\overline{A} \cdot \overline{B}$
1	0	0	1	0	1	1	1	0	0
1	1	0	0	1	0	0	1	0	0
0	1	1	0	0	1	1	1	0	0
0	0	1	1	0	1	1	0	1	1

Table 10: Truth table of Nature 7

● Nature 8: Law of Complementary

$A \cdot \overline{A} = 0$, $A+\overline{A} = 1$

The truth table is shown in Table 11.

A	$\overline{A}$	$A \cdot \overline{A}$	0	$A+\overline{A}$	1
1	0	0	0	1	1
0	1	0	0	1	1

Table 11: Truth table of Nature 8

● Nature 9: Unit Element Law

$A \cdot 1 = A$, $A+0 = A$

The truth table is given in Table 12.

A	1	0	A·1	A+0
1	1	0	1	1
0	1	0	0	0

Table 12: Truth table of Nature 9

● Nature 10

$A \cdot 0 = 0$, $A+1 = 1$

The truth table is shown in Table 13.

A	0	1	A·0	A+1
1	0	1	0	1
0	0	1	0	1

Table 13: Truth table of Nature 10

● Nature 11

$\overline{1} = 0$, $\overline{0} = 1$

This means that negation of the truth value "1" is "0" and negation of the truth value "0" is "1."

4. Identical equation

The basic nature has been explained in *3. Basic nature of Boolean Algebra.* Then let's solve identity problems. What is important here is to remember the basic nature only and forget all others. An identity, like the above basic rules, is an equation of two sides which work identically.

(Example 1)

$A+\overline{A} \cdot B = A+B$ ..... (1)

Expand the left member to the right:

$A+\overline{A} \cdot B = (A+\overline{A}) \cdot (A+B)$ ... ❶

$= 1 \cdot (A+B)$ ..... ❷

$= A+B$ ..... ❸

❶: Distributive Law

❷: Law of Complementary

❸: Commutative Law, Unit Element Law

Thus the equation (1) was proven to hold good by using the basic laws.

(Example 2)

$A \cdot (\overline{A}+B) = A \cdot B$..... (2)

Expand the left member to the right:

$A \cdot (\overline{A}+B) = A \cdot \overline{A}+A \cdot B$

$= 0+A \cdot B$

$= A \cdot B$

The identical equations (1) and (2) are important, called the Second Law of Absorption.

(Example 3)

$A\cdot B+A\cdot\bar{B}+\bar{A}\cdot B = A+B$ ..... (3)

Expand the left member to the right:

$A\cdot B+A\cdot\bar{B}+\bar{A}\cdot B = A\cdot(B+\bar{B})+\bar{A}\cdot B$ ... ❶

$= A+\bar{A}\cdot B$ ..... ❷

$= A+B$ ..... ❸

❶: Distributive Law

❷: Law of Complementary, Unit Element Law

❸: Second Law of Absorption

(Example 4)

$A\cdot B+\bar{A}\cdot C+B\cdot C = A\cdot B+\bar{A}\cdot C$ ..... (4)

Expand the left member to the right:

$A\cdot B+\bar{A}\cdot C+B\cdot C$

$= A\cdot B+\bar{A}\cdot C+B\cdot C\cdot(A+\bar{A})$ ..... ❶

$= A\cdot B+\bar{A}\cdot C+B\cdot C\cdot A+B\cdot C\cdot\bar{A}$ ..... ❷

$= \{A\cdot B+(A\cdot B)\cdot C\}+\{A\cdot C+(\bar{A}\cdot C)\cdot B\}$ ... ❸

$= A\cdot B+\bar{A}\cdot C$ ..... ❹

❶: Unit Element Law, Law of Complementary

❷: Distributive Law

❸: Commutative Law, Law of Association

❹: Law of Absorption

(Example 5)

$(A+C)\cdot(B+D)\cdot(B+C)\cdot(A+D) = A\cdot B+C\cdot D$ ..... (5)

Expand the left member to the right:

$(A+C)\cdot(B+D)\cdot(B+C)\cdot(A+D)$

$= \{(A+C)\cdot(A+D)\}\cdot\{(B+C)\cdot(B+D)\}$ .... ❶

$= (A+C\cdot D)\cdot(B+C\cdot D)$ ..... ❷

$= A\cdot B+C\cdot D$ ..... ❸

❶: Commutative Law, Law of Association

❷: Distributive Law

❸: Commutative Law, Distributive Law

5. Principle of duality

Now let's see an interesting law of Boolean algebra called the duality principle. It is explained as follows: A given identical equation will still be an equation when the following are exchanged simultaneously.

$\cdot \rightarrow +$

$+ \rightarrow \cdot$

$1 \rightarrow 0$

$0 \rightarrow 1$

Actually, of the basic rules of Boolean algebra discussed thus far, the duality principle holds true in each of a pair of two identical equations in Nature 2~11. The duality principle can also be confirmed by comparing identical equations in Examples 1 and 2.

$A+\bar{A}\cdot B = A+B$

$A\cdot(\bar{A}+B) = A\cdot B$

(Example 6)

$\bar{A}\cdot B+A\cdot\bar{B} = (A+B)\cdot(\bar{A}+\bar{B})$ ..... (6)

$(\bar{A}+B)\cdot(A+\bar{B}) = A\cdot B+\bar{A}\cdot\bar{B}$ ..... (7)

When equation (6) holds true, (7) too holds true. Let's first prove that (6) holds true:

$\bar{A}\cdot B+A\cdot\bar{B}$

$= (\bar{A}\cdot B+A)\cdot(\bar{A}\cdot B+\bar{B})$ ..... ❶

$= \{(A+\bar{A})\cdot(A+B)\}\cdot\{(\bar{A}+\bar{B})\cdot(B+\bar{B})\}$ ..... ❷

$= (A+B)\cdot(\bar{A}+\bar{B})$ ..... ❸

❶: Distributive Law

❷: Commutative Law, Distributive Law

❸: Law of Complementary, Unit Element Law

Then prove that equation (7) holds true:

$(\bar{A}+B)\cdot(A+\bar{B})$

$= (\bar{A}+B)\cdot A+(\bar{A}+B)\cdot\bar{B}$ ..... ❶

$= (A\cdot\bar{A}+A\cdot B)+(\bar{A}\cdot\bar{B}+B\cdot\bar{B})$ ..... ❷

$= A\cdot B+\bar{A}\cdot\bar{B}$ ..... ❸

❶: Distributive Law

❷: Commutative Law, Distributive Law

❸: Law of Complementary, Unit Element Law

Thus equation (7), a slightly modified version of (6) using the duality principle, proved also to be an identical equation.

When the principle is applied to identical equations verified in Examples 3~5, the following equations will be obtained:

From (3),

$(A+B)\cdot(A+\bar{B})\cdot(\bar{A}+B) = A\cdot B$ ..... (8)

From (4),

$(A+B)\cdot(\bar{A}+C)\cdot(B+C) = (A+B)\cdot(\bar{A}+C)$ .... (9)

From (5),

$A\cdot C+B\cdot D+B\cdot C+A\cdot D = (A+B)\cdot(C+D)$ .... (10)

Verify these equations yourself to determine that they hold true.

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